Tutorial 2
Inverter Layout

In this tutorial, a simple CMOS inverter layout will be drawn step by step. The HP 0.60 um technology design rule will be followed.

1. From the Library Manager, choose File then New and then Cellview
   (File --> New --> Cellview)

2. Enter cellname and choose layout cellview
   A dialog box will appear prompting you for the design library, cellname and cellview. Make sure that the library name corresponds to your design library, choose a name for your cell and choose Virtuoso as the design tool. The cellview will be selected as layout.
The LSW window and an empty Virtuoso will pop-up after you have entered the design name.

**LSW Window**

The Layer Selection Window (LSW) contains all the layers and their color formats that will be used to layout the circuitry.
We will start drawing the NMOS transistor. From the schematic, we know that this transistor size is W/L=1.2/0.6μ. The width of the transistor will correspond to the width of the active area. We will select the n-diffusion layer and draw a rectangular active area to define the transistor.

1. **Select nactive layer from the LSW**

![nactive layer from LSW](image)

2. From the Create menu in Virtuoso select Rectangle
   (Create --> Shape --> Rectangle )

3. **Draw the box**
   You are now in rectangle mode. Select the first corner of rectangle in the layout window (you may select any point within the window but try to select a point close to the origin), click once, and then move the mouse cursor to the opposite corner. Using the information bar, draw a box that is 3.6μ horizontal and 1.2μ vertical. All units are in micrometers by default. To simplify the drawing, a grid of half a lambda is used, that is the cursor moves in 0.15μ increments only. (Note, this number could be setup by click Options⇒Display⇒X snap spacing (0.15), Y X snap spacing (0.15). In most cases, this number has been setup by the system, you may not need to change it).

![Draw the box](image)

3. **It will be convenient if you have a ruler at hand.**
   From the Tools menu, click Create Ruler.
**The Gate Poly**

The second step is to draw the gate. We will use a vertical polysilicon rectangle to create the channel. Note that the length of the transistor channel will be determined by the width of this poly rectangle.

1. **Select poly layer from the LSW**

![Poly Layer](image)

In our case we need to draw the poly rectangle in the middle of the diffusion region.

3. **Draw poly rectangle**

![Poly Rectangle](image)

In our case we need to draw the poly rectangle in the middle of the diffusion region. Furthermore, according to design rules, poly must extend at least by 0.6u (2 Lambda) from the edge of the diffusion. Hence, the rectangle function is used to draw a poly rectangle that is 0.6u horizontal and 2.4u vertical.

**Making Active Contacts**

The next step is to make the active contacts. These contacts will provide access to the drain and source regions of the NMOS transistor.

1. **Select the cc (Active Contact) layer from the LSW.**
2. **Use the ruler to pinpoint a location 0.30u from the edges of diffusion.**
3. **Create a square with a width and height of 0.6u within the active area.**
4. From the Edit menu choose Copy
(Edit --> Copy)
You could choose to draw the second contact the same way as you have drawn the first one. However, copying existing features is also a viable alternative. The copy dialog box will pop-up as soon as you select the copying mode. For this operation the default values are appropriate. The Snap Mode is an interesting option. When this is in orthogonal setting the copied objects will move only along one axis. This is a good feature to help you avoid alignment problems.

5. Copy the contact
After you enter the copy mode, an object must be selected. Click in the contact, you'll notice that the outline of contact will attach to your cursor. Now move the object, and click when you are satisfied with the location.
Design rules state that the minimum contact to poly spacing must be 0.6\mu (2 lambda). You can use a ruler to pinpoint the location. Please note that you can interrupt any mode for placing a ruler (and zooming in and out). After you are finished (by hitting "ESC" key) you'll return to the mode you were in.

Now you have placed an active contact each into the source and drain diffusion regions of the transistor.

**Covering Contacts with Metal-1**

Active contacts in fact only define holes in the oxide (connection terminals). The actual connection to the corresponding diffusion region is made by the Metal layer.

1. Select layer *Metal-1* from the LSW

2. Draw two rectangles 1.2\mu wide to cover the contacts
Note that Metal-1 has to extend over the contact in all directions by at least 0.3μ (1 lambda).

**The N-Select Layer**

Each diffusion area of each transistor must be selected as being of n-type or p-type. This is accomplished by defining the "window" of n-type (or p-type) doping (implantation), through a special mask layer called n-select (p-select).

1. Select \textit{nselect} layer from the LSW.

2. Draw a rectangle extending over the active area by 0.6μ (2 lambda) in all directions.

This is the complete layout process of a NMOS transistor.

**PFET Layout**

**Drawing the P-Diffusion (Active)**

The next step is to draw the PMOS transistor. The basic steps involved in drawing the PMOS are the same.

1. Select \textit{pactive} layer from the LSW

2. Draw a rectangle 3.6μ by 1.2μ

You can use the cursor keys and the zoom function to find yourself a place to build the transistor. Make sure you leave enough separation between the NMOS and the PMOS. Note that the PMOS transistor will be surrounded by the N-well region.
These three steps are identical to the ones done for the NMOS.

1. **Draw the gate poly**

2. **Place the contacts**

3. **Cover contacts with Metal-1**
The P-Select Layer

As with the NMOS transistor, the p-type doping (implantation) window over the active area must be defined using the n-pelect layer.

1. Select *pselect* layer from the LSW

2. Draw a rectangle that extends over the active area by 0.6\( \mu \) (2 lambda) in all directions.

Drawing the N-Well

In this process, the silicon substrate is originally doped with p-type impurities. NMOS transistors can be realized on this p-type substrate simply by creating n-type diffusion
areas. For the PMOS transistors however a different approach must be taken: A larger n-type region (n-well) must be created, which acts like a substrate for the PMOS transistors. From the process point of view, the n-well is one of the first structures to be formed on the surface during fabrication. Here we chose to draw the n-well after almost everything else is finished. Note that the drawing sequence of different layers in a mask layout is completely arbitrary, it does not have to follow the actual fabrication sequence.

1. Select the *nwell* layer from the LSW

2. Draw a large n-well rectangle extending over the P-Diffusion

![Image](image.png)

The n-well must extend over the PMOS active area by a large margin, at least 1.8u (6 lambda)

**Placing the PMOS and NMOS transistors**

Usually, in CMOS digital circuit design, it is desirable to place the PMOS transistor directly on top of the NMOS transistor for a compact layout.

1. Select the PMOS transistor

First make sure that you are in selection mode. If you are in any other mode (like rectangle drawing mode) exit the mode by pressing "ESC". Now using the mouse, click and drag a box that covers your PMOS. If you were successful, all the objects within the PMOS would be highlighted as in the figure below:
2. From the menu *Edit* select the option *Move*
( Edit --> Move )

A window will pop-up similar to the copy window. This time we will have to change the *Snap Mode* option to *Anyangle* so that we can move the transistor freely.

3. Pick the reference point
We will be asked to find a reference point for the object to be moved. The cursor will practically grab the object from that reference point. Since we want an accurate placement, it is advisable to select a point for which alignment is simpler. The corner between the diffusion and the poly is a good place to grab the PMOS.
After we have picked the reference point, the outline of the shape will appear attached to the cursor and we will be able to move the shape around. Since the minimum distance from diffusion to the n-well edge is 1.8µ, the PMOS and NMOS have to be at least 3.6µ apart. We can place a ruler to help us aligning the two shapes and to measure the distance.

**Connecting the Output**

1. **Draw a Metal-1 rectangle between NMOS and PMOS drain region contacts**
Note that the minimum Metal-1 width is 0.9µ (3 lambda), thus narrower than the Metal-1 covering the contacts. Also note that the transistors are completely symmetric, the source and drain regions are interchangeable.
4. Place the transistor
You can drop the selected object (in this case consisting of the n-well, the p-active, poly and contacts) into its final location by clicking once on the left mouse button.
Connecting the Input

The next step will be to connect the gates of both transistors, which will form the input. To do this, we could use the `rectangle` command again, but this time we will use a different command, the `path` command. Throughout this tutorial, you will see that you typically have multiple options, commands or procedures available to create the same features in the layout. Please become familiar with as many of such options as possible.

1. Select `poly` layer from the LSW

![poly dq](image)

2. From the Create menu select Path

  (Create --> Shape --> Path)

The path options box will pop up:

![Path options box](image)

In the `path` mode you can draw lines (or paths) with the selected layer. The width of the drawn line can be adjusted; the default is the minimum width of the selected layer.

3. Start path

To start the path, click on the middle of the PMOS poly extension. You'll see a ghost line appear. Move this ghost line to the NMOS poly extension.
4. Double click to finish path

A single click will finish a line segment and let you continue drawing, a double click will finish the path.

Making a Metal-1 connection for the Input

In this design, we want that the layer for the input signal is Metal-1. Therefore we have to make a connection from the poly layer to the Metal-1 layer.

This connection can be done manually by drawing a poly contact layer between Metal-1 and poly, but we will use the path command to automatically add the contacts.

1. Starting from the poly line connecting the gates, start drawing a horizontal poly path

2. On the Path Options dialog box, click on Change To Layer and switch to Metal1
This will automatically add a contact to the end of the current path. Note that this will still be a ghost line. You can place the contact at a certain location by clicking once, thereafter the path will continue using the new layer.

**Power Rails**

Now that our transistors are placed and connected, we will have to add Power and Ground rails. Usually a layout consists of a large number of cells, all of which need power and ground connections. Therefore it is common to design cells such that they will have one continuous, wide power and ground connection when placed side by side.

In this layout, the horizontal power and ground lines are drawn in Metal-1.

1. **Draw the Power Rail in Metal-1 above the PMOS**

2. **Draw the Ground Rail in Metal-1 below the NMOS**

Note the active region is 0.9um (3 lambda) away from the power or ground rail.
P-Substrate Contact

The substrate on which the transistors are built must be properly biased. The way to do this is to add substrate contacts. The NMOS transistors are build on a p-type substrate, we will have to create a p-type substrate contact.

1. **Draw a P-select square next to the NMOS transistor.**
   Since the contact will be made to p-substrate, the contact area will have to be p-type.

2. **Draw a P-active square inside the P-select area.**
   This will define the active area of the substrate contact. Make sure that you are not violating any design rules associated with active area spacing.
3. Draw the active contact square inside the p-type active area.

4. Make a metal connection to ground, covering the entire substrate contact.
Note that the substrate contact can also be created and placed as an instance, instead of drawing every item separately. This alternative approach will be demonstrated in the next step, for the n-well contact.

Make sure to connect the Power Rail and the Ground rail to the source contact of the PMOS and to that of NMOS, respectively.
N-Substrate Contact

The PMOS transistor was placed within the n-well, this well also has to be biased with the VDD potential. This will be done with an n-type substrate contact.

There are two ways to layout the substrate contact. One is to design every layer manually. The other way is to get the substrate contact instance from the library.

1. From the menu Create select option Instance (Create --> Instance) This will pop-up the instance options menu.

You'll have to provide a cell name and library here. It may be the case that you already know the cell name and cell view, but in this case it is better to Browse in your library to find the appropriate cell.

NCSU_TechLib_hp06 → ntap (Note, not NTAP)

Using the same operation, to place the p-substrate contact ptap.

2. Move the instance to the desired location.
3. Place the instance.

Once satisfied, you can click to place the instance. You'll remain in the instance mode after you have placed the instance, press "ESC" to go back to selection mode again.

4. Extend the N-Well to cover the N-Substrate contact.

5. Make the Power connection

Connect the N-substrate contact to Vdd, P-substrate contact to Gnd.
**Design Rule Checking**

The layout must be drawn according to strict design rules. After you have finished your design, an automatic program will check each and every feature in your design against these design rules and report violations. This process is called Design Rule Checking (DRC).

Our design is finished; we must now perform a Design rule Check to see if we have any errors.

1. **From the menu Verify select option DRC** (Verify --> DRC), which will pop-up the DRC options dialog box.

![DRC options dialog box]

2. **Start DRC**

The default options for the DRC are adequate for most situations. DRC results and progress will be displayed in the CIW. You'll have to check the results from the CIW.