

Tutorial 1 *

Cadence Schematic Capture and Circuit Simulations

Background

The CADENCE environment allows access to libraries containing icons of basic circuit components and the ability to place and connect these devices into the form of a circuit within a schematic editor. In addition, the default values of the properties of the various elements can be edited and altered to fit the requirements of the actual system under design. Files can then be extracted from the graphical circuits into forms compatible with Spectra or Spice circuit simulators. The simulators can then be called to compute and plot the various waveform results. Once the designer is satisfied with the operation of the circuit, the schematic can then be put into the form of a symbol and used as a component in higher-level circuits. Finally, at this higher level, the overall design can be simulated and the results plotted. If it is found that the simulated results do not meet the technical requirements, it is possible to go back through various layers of the design and alter properties at each stage before continuing additional simulations. This iterative interaction is a powerful tool that helps the circuit designer to quickly test design concepts and debug circuits.

Basic Operations

In these exercises, you are expected to learn:

1. **Use the schematic composer to connect a circuit using components from the North Carolina State University (NCSU) Analog Library.**
2. **Simulate the design and plot the stimulus and the outputs.**
3. **Change the properties of devices within the design and iterate to reach a suitable conclusion.**

Start the Cadence under our Linux System:

1. Logon to the Linux system using your **ID** and **PWD**.
2. Open a terminal window, and type **xhost +**
3. Open a new terminal window,
telnet tyr (or tyr.cems.uvm.edu)
type in your **ID** and **PWD**
set the display mode as **“ansi”**
type: **setenv DISPLAY machine_name:0**

(On the monitor, you can find a paper stick which labels the name of the computer that you are using)

You need to create a new directory

```
mkdir ee221
```

Go to the new directory

```
cd ee221
```

Then copy two files

```
cp /usr/local/apps/cadence2009/ic/example/.cdsinit ./  
cp /usr/local/apps/cadence2009/ic/example/cds.lib ./
```

when use **ls -a** command, you should see these two files in the directory.

After copying files, please use command

chmod 755 cds.lib

chmod 755 .cdsinit

These commands will change the mode of two files, and enable them to be modified later.

Now you are ready to start Cadence program for circuit design.

1. The first step in this assignment is to bring up the Cadence “Command Interpreter Window” (CIW) by opening a window and typing:

virtuoso

This will open the CIW. Choose **Tools -> Library Manager...** from the CIW Menu.

2. In the Library Manager, use the left button of the mouse to select **File → New → Library**. This will result in a new window where you may create a “library” by filling in a name. In Cadence, a library is nothing more than a directory in your home account.
3. Once you have filled in the name of your new library, you should fill in the selection “**Attach Library to Technology library**”. Select “**NCSU_TechLib_HP06**”, which corresponds to a HP 0.6 micron technology, and then enter “**OK**”.
4. Go to the Library Manager and highlight your new library. Select **File → New → Cell View**. This will bring up a new window, “**Create New File**”. You will have to give the cell a name (i.e. inverter) by filling in the blank space to the right of “**Cell Name**”. The view will read “**schematic**”. Note that the “**Application**” is automatically set to “**Schematics L**”. Then select “**OK**”, which will bring you into a new window, “Virtuoso Schematic Editing”.

You may see a warning about getting a license. Simply click **YES** to ignore this warning or **Always** to never see it again.

5. In the Virtuoso window, you will want to “**Add**” (components, wire, pins, etc) circuit elements; “**Edit**” (Move, Copy, Delete, etc); “**Design**” (Check and Save, etc.); and under “**Tools**”, use the **Analog Environment** to perform analysis on the design.
 - **Adding Components:** When you select **Add → Instance**, you will bring up a window, “**Add Instance**”, referencing the “**Library**”, **NCSU_Analog_Parts**. At this point you should select the button, “**Browse**”, which will bring up a new window, “**Library Browser – Add Instance**” to allow you to choose the part that you need, **nmos** (an NMOS transistor), **pmos** (a pMOS transistor), **vdc** (a DC power supply), **vpulse** (a voltage pulse generator), or **res** (resistor). Supply_Nets: **Vdd** and **GND**. Just make sure that you select the “**View**”, “**Symbol**”. This, in turn will bring up a new window, “**Add Instance**” that will allow you to specify the

parameters of the instance that you have chosen. Be sure to fill in the proper values that you expect to use in your design.

In this design, we will implement a CMOS inverter, so you should add one PMOS and one NMOS transistors.

- **Placing Components:** Once you have selected your components, you can place it in the Virtuoso Schematic window by using the mouse to locate the icon where you want it deposited and then striking the left mouse button. Once you have deposited a particular component, just strike the “**Esc**” key.
- **Connecting With Wires:** Connections are made between components using **Create → Wire (narrow)**. Use the left mouse button to attach one end of the wire to a node of the component. The wire can then be routed to the next component and attached in a like manner. Again, strike the “**Esc**” key to terminate this operation. (It is recommended that you always have wire between components rather than directly connecting a node of one component to the node of a second. The reason is that you can only use wires to display voltages. Nodes are restricted to current measurements).
- **Moving Objects:** To move an object, go to **Edit → Move**. Then centering the cursor over the object until you get a rectangle with sides appearing. Then click with the leftmost button of the mouse and you will get a copy of the object. You can then move the object to any point in the window. Once the object is located where you wish it to be newly located, just strike the **Esc** key and it will be deposited at that location.
- **Selecting Objects:** To change the properties or delete object, you must first select them using the mouse and the mouse’s leftmost button. You first envision that you want to locate a rectangle completely enclosing the object, including its nodes. Then place the cursor to the left-hand lower corner of the envisioned rectangle, press the leftmost button, and without releasing the button, stretch a diagonal path to where envision that upper rightmost corner of the envisioned rectangle must be. This will result in a rectangle surrounding the object, which indicates its selection.

Properties: One of the purposes of selecting an object is to edit its properties. After selection, the properties may be altered with **Edit → Properties → Object**. This will bring up a window, “**Edit Object Properties**”. Once you have changes the device properties, strike “**Apply**” and then “**OK**”.

In this design example, we will set the transistor sizes to be:

PMOS transistor: width/length=3.6u/600n

NMOS transistor: width/length=1.8u/600n

You may also need to specify the MOS transistor **model name**. For instance, the PMOS device in the model file is defined as *hp14tbP* and the NMOS device name is *hp14tbN*.

For the DC power supply voltage source, its value is set to be 3.3 (v)

The property of voltage source “**Vpulse**” is a little complex. Several parameters should be set:

Voltage 1:	0
Voltage 2:	3.3
Delay time:	1n
Rise time:	1n
Fall time:	1n
Pulse width:	9n
Period:	20n

- At the output terminal, an output pin is needed when no other load device exists. At the top of the schematic window, click an icon called **Pin**. A new window “**add pin**” is created. Then fill in the **Pin Name**, for instance “**Inv_out**”, the pin **Direction** is set as “**output**”.
- **Deleting Objects:** A second reason for selecting an object is to delete it. After selection, this is done with **Edit → Delete**. If you immediately decide you have made a mistake, you can undo the deletion with **Edit → Undo**.
- **Saving and Simulation:** Once you have completed a design, you may simulate it to see if you get the results you expect. However, you must first have the circuit checked and saved. This is done with **Check → Current View**. After this operation, check in the CIW widow to see if you have any errors. If not, you will see a message, “Schematic check completed with no errors”. Now to set up for simulation.

6. Simulate the Schematic with Spectre within Analog Artist

From the Schematic Window menu, select **Launch -> ADE L**. You may get another message saying that the license need to be upgraded. Simply click Ok to proceed. A window will pop-up. This window is the Analog Design Environment Window.

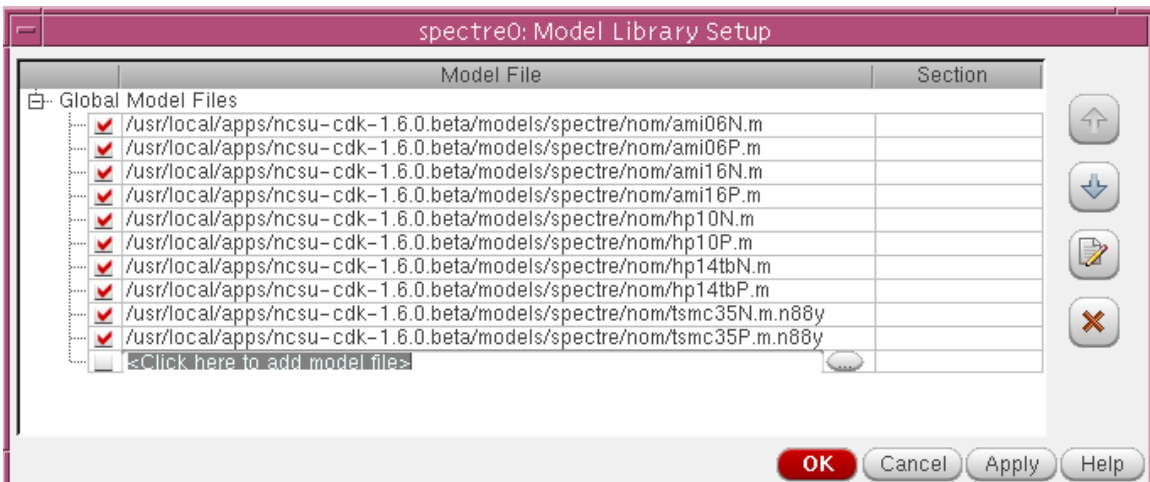
In the Analog Circuit Design Environment window, you will have to perform several tasks. First, you will have to tell the program where the models for your transistor devices are located. Next, you will have to select the form of analysis and the outputs that you wish to observe. Finally, you will ask for a netlist and a graphical display of the results of the analysis. The particular steps and their order that you must follow while in this window are given in the bullet list below.

Choose a Simulator

By default the **Spectre** simulator is chosen. If you want to change it, from the Analog Artist menu, select **Setup -> Simulator/Directory/Host**. Your simulation will run in the specified Project Directory. You may choose any valid pathname and filename that you like. Cadence generates many temporary files for simulation, so you do not want to leave them in your home directory.

Choose Model Library

From the Analog Artist menu, select **Setup ->Model Library....** Add model files as below



- The next step is to select form of analysis. Let's assume it will be a transient response, an output voltage or current as a function of time. This selection is made through **Analysis -> Choose**. Select the button, "**tran**" and type in the stop time in the blank space to the right of "**Stop Time**". (e.g. 200n for 200 nanoseconds). Note, there is no space between the characters.
- You must now select the output you wish to follow. This is begun with **Outputs -> To Be Plotted -> Select on Schematic**. You now go back to the Virtuoso window and use the leftmost mouse to select either the voltage of current you wish to follow. If you select a node, you will measure current; if you select a wire between tow nodes, you will measure voltage. If you select current, the node will be encircled with an ellipse; if you select voltage, the wire will become highlighted.
- The final step is to perform the analysis. This is done by selecting **Simulation -> Run**. You may watch the CIW to see if you are going to be successful. If you are not successful, you need to correct error in your design.

- If your simulation is successful, you will get a window, “**Waveform Window**”, showing the signal traces. These are manipulations that you can do within this window on the signal.

Appendix:

- A. You can create a symbol from the schematic composer after you have completed the connection of a circuit: **Design → Cellview → From Cellview**. The circuit may or may not contain power supplies or grounds, but, instead have pins with the proper directionality: input or output.
- B. The symbol can then be placed in a higher level schematic design that is used as a “testbench”. The circuit, excluding the symbol, may contain only a capacitive load; optionally, a DC voltage source to define the value of the ground and Vdd you potential used in your symbol as well as any other pulse generators whose voltage values, rise times, fall times, and periods will have to be specified. These connections will have to be made with wires to the symbol and the wires whose output you will later wish to plot will have to be labeled so that they can be referenced by the simulator.
- C. In iteratively debugging a schematic, you may have to go in and changes the circuit substantially. You can save the state of the Analog Artist Simulation window (the nodes where you wan the voltage measured, the type of analysis, etc.) by using **Session → Save State**. After modifying properties of the devices or symbols in your circuit, this state can be reloaded with **Session → Load State**.
- D. **Session → Reset** will allow you to select devices within the Schematic Composer and to edit their properties.
- E. In the Schematic Composer, you can click on your symbol and edit it by **Design → Hierarchy → Descend Edit**, which will open a Schematic Composer window with your original circuit in it.
- F. In this new Schematic Composer that results, you can changes the properties of your transistors with **Edit → Properties → Object**.
- G. You may “ascend” back to the original design by either **Design → Return to Top** or iteratively using **Design → Return**. You may have to retrieve the test bench schematic by using **Design → Open**.
- H. In the Waveform window, it is useful to use **Axis → To Strip to separate signal waveforms**.
- I. On the left side of the Waveform window, there are some icons including “**Crosshair Marker A**” and “**Crosshair Marker B**”. When you put these two markers on waveforms, the distance between the markers will be given at the bottom of the window. Please measure the propagation delay of the inverter that you just implemented.

Assignment:

1. Implement three CMOS inverters using HP0.60u AMOS14TB technology.

The inverters sizes are:

1). Inverter 1:

PMOS: W/L=3.6u/600n

NMOS: W/L=1.8u/600n

2). Inverter 2:

PMOS: W/L=7.2u/600n

NMOS: W/L=3.6u/600n

3). Inverter 3:

PMOS: W/L=1.8u/600n

NMOS: W/L=900n/600n

The voltage sources are the same as those introduced in the tutorial part.

2. Implement the schematic of a two-input NOR gate

$$f = \overline{a + c}$$

Run the transient analysis: (You should select the proper voltage sources with reasonable parameters).

Transistor sizes:

PMOS: W/L=3.6u/600n

NMOS: W/L=1.8u/600n

Report:

1. Inverter and NOR gate Schematics
2. The transient analysis waveforms for each gate
3. Draw a table and list each inverter's propagation delay