Tutorial 4
Create Custom Layouts

In tutorial 3, we did the circuit layout layer by layer manually. In this tutorial, we will learn how to use program Layout XL to create transistors layout automatically. This program will make the circuit layout not so scary☺!

Procedures:

- In the schematic window, now click Tools->design synthesis -> Layout XL

This opens up the virtuosoXL Layout editing window and the Layer select window (LSW)

In order to show the raw netlist, In your Layout window click Design-> Gen from source.
make the following changes in the layout generation form;
1. DESELECT boundary.
2. Change all default Layer/Master to
3. Your width should be 3.6
4. Select text display for pin label shape (you can reduce the font size to 0.5 in display pin name option.)
5. click OK. (Top left corner).
Now, change the display setting of your layout window by clicking options ->
display.
1. Click Defaults.
2. Then change your X Snap and Y Snap spacing to 0.05 and Apply, OK.
   (This is important so as to reduce the DRC errors).

Now we start the actual Layout Editing. The Hotkeys are:

- \textit{i}: Add instances
- \textit{q}: Edit properties
- \textit{r}: Add rectangles
- \textit{p}: Add path
- \textit{P}: Add Polygon
- \textit{ctrl+p}: Add a pin
**l**: Label a wire

**z**: Zoom in

**Z**: Zoom out by 2X

**ctrl+z**: Zoom in by 2X

**f**: fit the layout in your layout window

**right mouse button**: repeat last command

- Hit "ESC" to come out of any mode.

Steps involved:

1. Drag a rectangle over a component and move it (hotkey m)
   (Layout XL has a helpful feature that when a component is selected in layout, the corresponding element in schematic is highlighted).

2. select poly in LSW and join the gate of Nmos and Pmos. (hotkey p).

3. select metal1 in LSW and make connection to output, Vdd! and gnd! rails
   (please note that when you are moving the pins vdd! and gnd! both the label and the small rectangle should be selected and moved, else it gives errors as unlabelled pins and labels without a pin...).

4. for joining input we need a via from poly to metal 1, which is:
   select poly in LSW.
   hit p for path, and make some path over the poly connection and single click.
   go to the create path window and do "change to layer -metal1"
   (it automatically places a via and switches to metal1). join this to inv_in.
After making the initial connections the drawing will look like this (or some variant of this as the example puts little emphasis on area optimization in the current layout).

Hey, but don’t you think that we are missing something?? wheres the substrate (bulk) terminals for the pmos and nmos. as it figures out we have to manually place them...

1. hit i or create->instance browse and select NCSU_TechLib_hp06 -> "ntap" (and NOT NTAP).
2. place it in PMOS abutting the pactive(orange outline) rectangle.
3. create a rectangle of nwell covering the ntap. (hit <esc>, select nwell in LSW and press r.)
4. hit i and select NCSU->TechLib_hp06->ptap.
5. place it in NMOS abutting nactive. (no nwell fill is required).
6. bias the substrate by connecting it to vdd! or gnd!.

- Check and save your design

Before saving the design, we hope to make sure that the design has conformed to the design rules. As careful as one might be, it is very hard for a designer to avoid all the design rule errors. To perform the design rule checking, click on Verify -> DRC... in the layout window. A pop up dialogue box will appear.

<table>
<thead>
<tr>
<th>DRC</th>
</tr>
</thead>
<tbody>
<tr>
<td>OK</td>
</tr>
</tbody>
</table>

- Checking Method
  - flat
  - hierarchical
  - hier w/optimization

- Checking Limit
  - full
  - incremental
  - by area

- Switch Names
  - Coordinate
  - Set by Cursor

- Run-Specific Command File
  - Limit Rule Errors
  - Limit Run Errors

- Inclusion Limit
  - 1000

- Join Nets With Same Name
  - Limit Rule Errors
  - Limit Run Errors

- Echo Commands
  - Off

- Rules File
  - divaDRC.rules

- Rules Library
  - SU_TechLib_hp06

- Machine
  - local
  - remote
  - Machine

- Use Error Database
  - Off

For a small circuit like an inverter, it is OK just to run the DRC in the flat mode since the running time is short. For a big layout, however, it is wise to run the DRC in a hierarchical mode. In general, hierarchical mode is faster than flat mode, especially for a large layout composed of iterative structures. However, hierarchical DRC might not be accurate in some rare cases. Thus it is a good practice to check a big circuit with hierarchical DRC first and then
run a flat DRC by the end. Click on the OK button and the Diva DRC tools will be invoked the check the design and reports the errors in the CIW.

In this case, the CIW above shows that there is no error found in the DRC process. If, however, there is any error reported, the layout will be marked and CIW will indicate what kind of violations there are. You can then modify the layout and run the DRC again till there is no DRC errors.

After the cell has been checked, click on Design -> Save... in the layout window to save your design.

Extract the Layout
When you are done creating the layout, save the design, and then select Verify-> Extract… . Make sure Extract Method is set to “flat”, Echo Commands is unchecked. Click Ok.
You should also notice that a new cell view has been created, called “extracted”. Open the extracted view and examine it. You’ll notice that the layers in the extracted view are like the ones in the layout view (metal1, poly, etc.) except that they’re in the “net” purpose (“nt”) rather than the “drawing” purpose (“dg”). (The pin rectangles that you created, however, will still be in the “drawing” purpose). Cadence uses the different “purposes” to distinguish shapes that are meant for different things. Here, for example, the net purpose is used to indicate that the shape is showing the location for a net, rather than being the actual shape that should be used to generate the mask-patterns for manufacturing.

Perform an LVS Check
LVS means Layout vs. Schematic. It is used to check the layout matches the original circuit in the schematic.
Now, in the layout window, select Verify->LVS… .
NOTE: If you are running LVS multiple times, you may see a dialog box warning you that the “LVS Run directory does not match the Run Form”. If you select the “Form Contents” option, then the LVS dialog will be updated with the name of the cell that you are currently editing. Otherwise, if you choose the “Run Directory” option, the dialog will be updated with the values from the last LVS run.
Once the LVS is done, click Output to find out if there is any mismatch between layout and schematic. If there is, that means the layout is not done correctly, corrections are needed.

**Our first cell is ready, now lets make a few million of these :-) .**

**Assignment:**

Implement the following logic: $S = \overline{A + BC}$

Including Schematic and Layout

The transistor sizes are the same as those in the inverter in the 1st lab.