

Model*Sim*

SE

Tutorial

Version 5.5d

Published: 22/Aug/01

The world's most popular HDL simulator

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Introduction

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Software versions

This documentation was written to support ModelSim SE 5.5d for UNIX and Microsoft Windows 95/98/Me/NT/2000. If the ModelSim software you are using is a later release, check the README file that accompanied the software. Any supplemental information will be there.

Although this document covers both VHDL and Verilog simulation, you will find it a useful reference even if your design work is limited to a single HDL.

ModelSim's graphic interface

While your operating system interface provides the window-management frame, ModelSim controls all internal-window features including menus, buttons, and scroll bars. The resulting simulator interface remains consistent within these operating systems:

- SPARCstation with OpenWindows, OSF/Motif, or CDE
- IBM RISC System/6000 with OSF/Motif
- Hewlett-Packard HP 9000 Series 700 with HP VUE, OSF/Motif, or CDE
- Linux (Red Hat v. 6, 7 or later) with KDE or GNOME
- Microsoft Windows 95/98/Me/NT/2000

Because ModelSim's graphic interface is based on Tcl/Tk, you also have the tools to build your own simulation environment. Easily accessible preference variables and configuration commands, simulator preference variables, and graphic interface commands give you control over the use and placement of windows, menus, menu options and buttons.

Standards supported

ModelSim VHDL supports both the IEEE 1076-1987 and 1076-1993 VHDL, the 1164-1993 *Standard Multivalued Logic System for VHDL Interoperability*, and the 1076.2-1996 *Standard VHDL Mathematical Packages* standards. Any design developed with ModelSim will be compatible with any other VHDL system that is compliant with either IEEE Standard 1076-1987 or 1076-1993.

ModelSim Verilog is based on the IEEE Std 1364 *Standard Hardware Description Language Based on the Verilog Hardware Description Language*. The Open Verilog International *Verilog LRM version 2.0* is also applicable to a large extent. Both PLI (Programming Language Interface) and VCD (Value Change Dump) are supported for ModelSim PE and SE users.

In addition, all products support SDF 1.0 through 3.0, VITAL 2.2b, VITAL'95 - IEEE 1076.4-1995, and VITAL 2000.

Assumptions

We assume that you are familiar with the use of your operating system. You should be familiar with the window management functions of your graphic interface: either OpenWindows, OSF/Motif, CDE, KDE, GNOME, or Microsoft Windows 95/98/Me/NT/2000.

We also assume that you have a working knowledge of VHDL and Verilog. Although *ModelSim* is an excellent tool to use while learning HDL concepts and practices, this document is not written to support that goal.

Where to find our documentation

ModelSim documentation is available from our website at www.model.com/support/documentation.asp or in the following formats and locations:

Document	Format	How to get it
<i>Start Here for ModelSim SE</i> (installation & support reference)	paper	shipped with <i>ModelSim</i>
	PDF	select Main window > Help > SE Documentation ; also available from the Support page of our web site: www.model.com
<i>ModelSim SE Quick Guide</i> (command and feature quick-reference)	paper	shipped with <i>ModelSim</i>
	PDF	select Main window > Help > SE Documentation , also available from the Support page of our web site: www.model.com
<i>ModelSim SE Tutorial</i>	PDF, HTML	select Main window > Help > SE Documentation ; also available from the Support page of our web site: www.model.com
<i>ModelSim SE User's Manual</i>	PDF, HTML	select Main window > Help > SE Documentation
<i>ModelSim SE Command Reference</i>	PDF, HTML	select Main window > Help > SE Documentation
<i>ModelSim Foreign Language Interface Reference</i>	PDF, HTML	select Main window > Help > SE Documentation
<i>ModelSim Command Help</i>	ASCII	type <code>help <command_name></code> at the prompt in the Main window
Tcl Man Pages (Tcl manual)	HTML	select Main window > Help > Tcl Man Pages , or find <code>contents.htm</code> in <code>\modeltech\docs\html</code>
technotes	ASCII	select Main window > Help > Technotes , or located in the <code>\modeltech\docs\technotes</code> directory

Technical support and updates

The Model Technology web site includes links to support, software updates, and many other information sources.

Support

www.model.com/support/default.asp

Customers in Europe should contact their distributor for support. See www.model.com/contact_us.asp for distributor contact information.

Updates

www.model.com/products/release.asp

Latest version email

Place your name on our list for email notification of news and updates.
model.com/support/register_news_list.asp

Before you begin

Preparation for some of the lessons leaves certain details up to you. You will decide the best way to create directories, copy files and execute programs within your operating system. (When you are operating the simulator within ModelSim's GUI, the interface is consistent for all platforms.)

Additional details for VHDL, Verilog, and mixed VHDL/Verilog simulation can be found in the *ModelSim User's Manual* and *Command Reference*. (See "[Where to find our documentation](#)" (T-7).)

Examples show Windows path separators - use separators appropriate for your operating system when trying the examples.

Command, button, and menu equivalents

Many of the lesson steps are accomplished by a button or menu selection. When appropriate, VSIM command line (PROMPT:) or menu (MENU:) equivalents for these selections are shown in parentheses within the step. This example shows three options to the **run -all** command, a button, prompt command, and a menu selection.



(PROMPT: run -all)

(MENU: Run > Run -All)

Drag and drop

Drag and drop allows you to copy and move signals among windows. If drag and drop applies to a lesson step, it is noted in a fashion similar to MENUS and PROMPTS with: DRAG&DROP.

Command history

As you work on the lessons, keep an eye on the Main transcript window. The commands invoked by buttons and menu selections are echoed there. You can scroll through the command history with the up and down arrow keys, or the command history may be reviewed with several shortcuts at the ModelSim/VSIM prompt.

Shortcut	Description
click on prompt	left-click once on a previous ModelSim or VSIM prompt in the transcript to copy the command typed at that prompt to the active cursor
his or history	shows the last few commands (up to 50 are kept)

Reusing commands from the Main transcript

ModelSim's Main transcript can be saved, and the resulting file used as a DO (macro) file to replay the transcribed commands. You can save the transcript at any time before or during simulation. You have the option of clearing the transcript (File > Clear Transcript) if you don't want to save the entire command history.

To save the contents of the transcript select **File > Save Transcript As** from the Main menu.

Replay the saved transcript with the **do** command:

```
do <do file name>
```

For example, if you saved a series of compiler commands as *mycompile.do* (the .do extension is optional), you could recompile with one command:

```
do mycompile.do
```

▶ **Note:** Neither the prompt nor the Return that ends a command line are shown in the examples.

Lesson 1 - Creating a Project

The goals for this lesson are:

- Create a project

A project is a collection entity for an HDL design under specification or test. Projects ease interaction with the tool and are useful for organizing files and simulation settings. At a minimum, projects have a work library and a session state that is stored in a .mpf file. A project may also consist of:

- HDL source files or references to source files
- other files such as READMEs or other project documentation
- local libraries
- references to global libraries

For more information about using project files, see the *ModelSim User's Manual*.

- 1 Start ModelSim with one of the following:

for UNIX at the shell prompt:

```
vsim
```

for Windows - your option - from a Windows shortcut icon, from the Start menu, or from a DOS prompt:

```
modelsim.exe
```

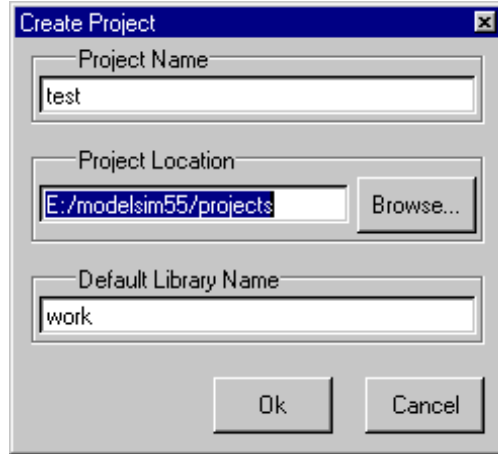
- 2 Upon opening ModelSim for the first time, you will see a Welcome to ModelSim dialog box. (If this screen is not available, you can enable it by selecting **Help > Enable Welcome** from the Main window. It will then display the next time you start ModelSim.)



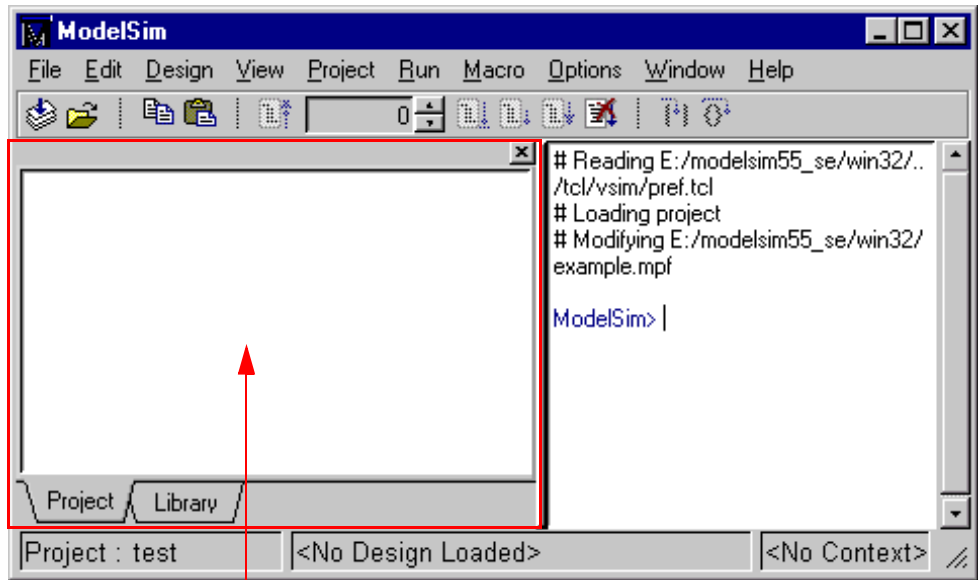
Select **Create a Project** from the Welcome to ModelSim dialog box. Or select **File > New > Project** from the ModelSim Main window.

Selecting **Create a Project** opens the Create Project dialog box.

- 3 In the Create Project dialog box, enter "test" as the Project Name and select a directory where the project file will be stored. Leave the Default Library Name set to "work."

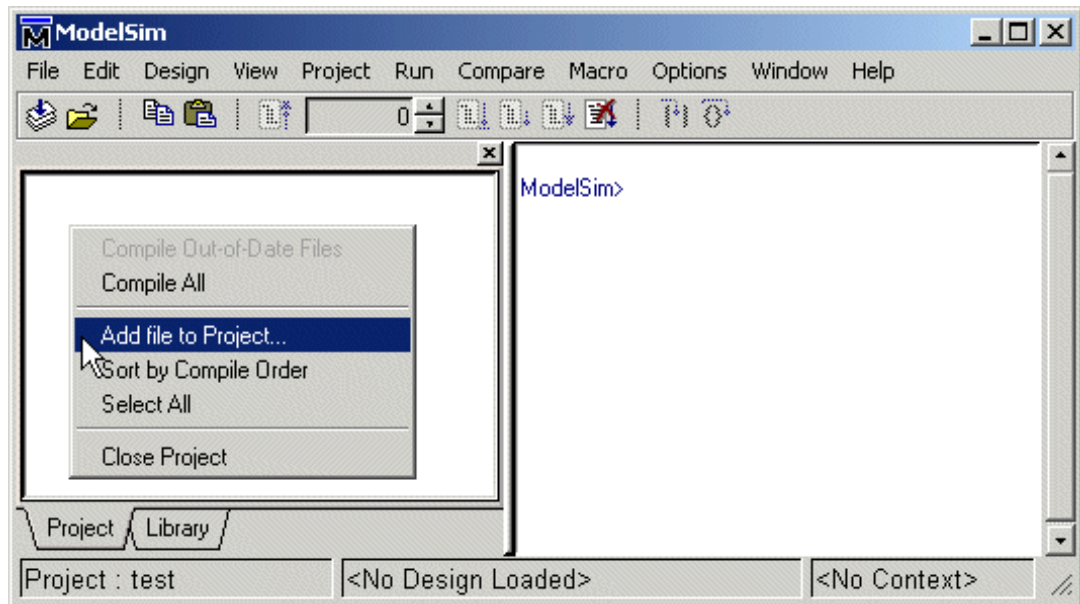


- 4 Upon selecting OK, you'll see the Main window with Project and Library tabs. Notice too that the Project name is shown in the status bar below the Workspace.

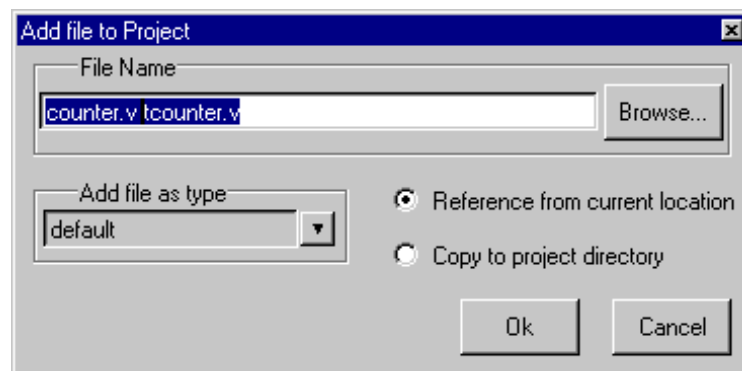


Workspace

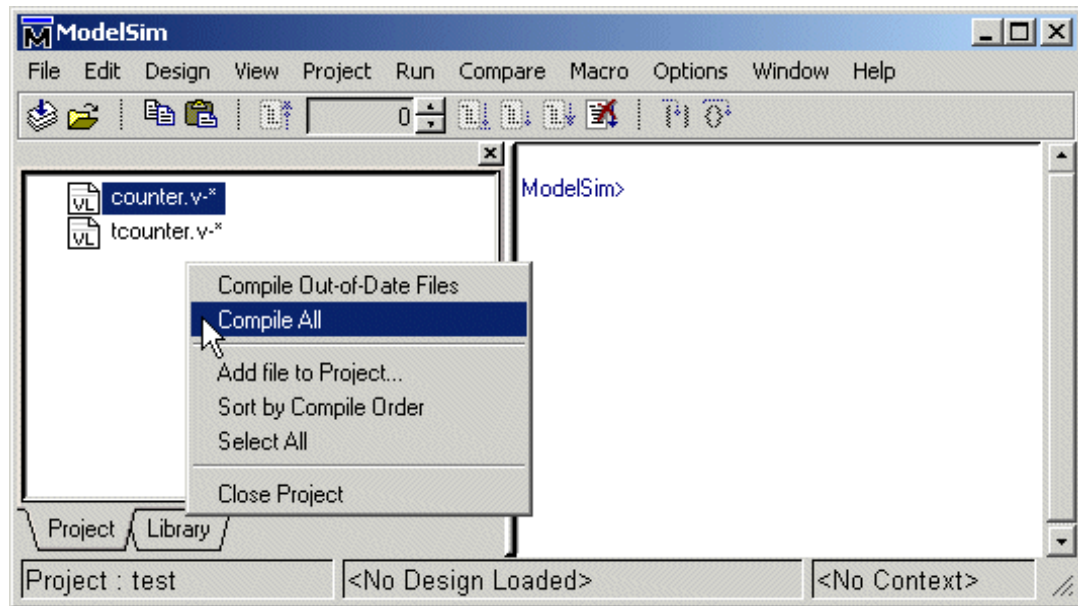
- 5 The next step is to add the files that contain your design units. Click your right mouse button (2nd button in Windows; 3rd button in UNIX) in the Project page of the Workspace, and select **Add File to Project**.



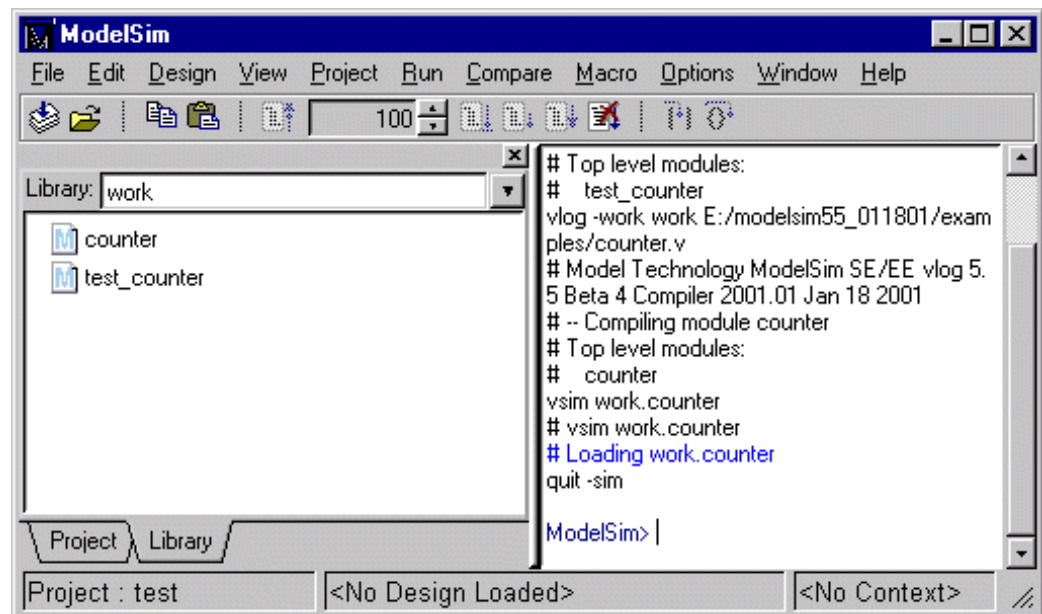
- 6 For this exercise, we'll add two Verilog files. Click the **Browse** button in the Add file to Project dialog box and open the examples directory in your ModelSim installation. Select *tcounter.v* and *counter.v*. Select **Reference from current location** and then click OK.



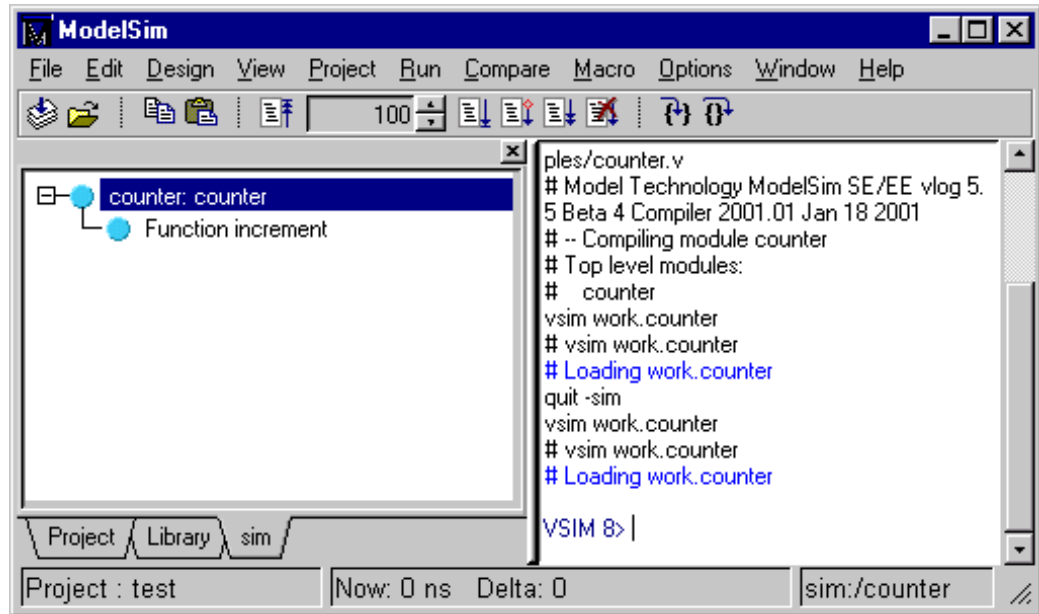
- 7 Right click in the Project page and select **Compile All**.



- 8 The two files are compiled. Click on the Library tab and you'll see the compiled design units listed. If you don't see the design units, make sure the Library: field shows "work."



- 9 The last step in this exercise is to load one of the design units. Double-click *counter* on the Designs page. You'll see a new page appear in the workspace that displays the structure of the *counter* design unit.



At this point, you would generally run the simulation and analyze or debug your design. We'll do just that in the upcoming lessons. For now, let's wrap up by ending the simulation and closing the project. Select **Design > End Simulation** and after confirming you want to quit simulating, select **File > Close > Project**.

Lesson 2 - Basic VHDL simulation

The goals for this lesson are:

- Create a library
- Compile a VHDL file
- Start the simulator
- Learn about the basic *ModelSim* windows, mouse, and menu conventions
- Run *ModelSim* using the **run** command
- List some signals
- Use the waveform display
- Force the value of a signal
- Single-step through a simulation run
- Set a breakpoint

The project feature covered in Lesson 1 executes several actions automatically such as creating and mapping work libraries. In this lesson we will go through the whole process so you get a feel for how *ModelSim* really works.

Preparing the simulation

- 1 Start by creating a new directory for this exercise (in case other users will be working with these lessons). Create the directory, then copy all of the VHDL (.vhd) files from `\<install_dir>\modeltech\examples` to the new directory.

Make sure the new directory is the current directory. Do this by invoking *ModelSim* from the new directory or by selecting the **File > Change Directory** command from the *ModelSim* Main window.

- 2 Start *ModelSim* with one of the following:

for UNIX at the shell prompt:

```
vsim
```

for Windows - your option - from a Windows shortcut icon, from the Start menu, or from a DOS prompt:

```
modelsim.exe
```

- ▶ **Note:** if you didn't add *ModelSim* to your search path during installation, you will have to include the full path when you type this command at a DOS prompt.

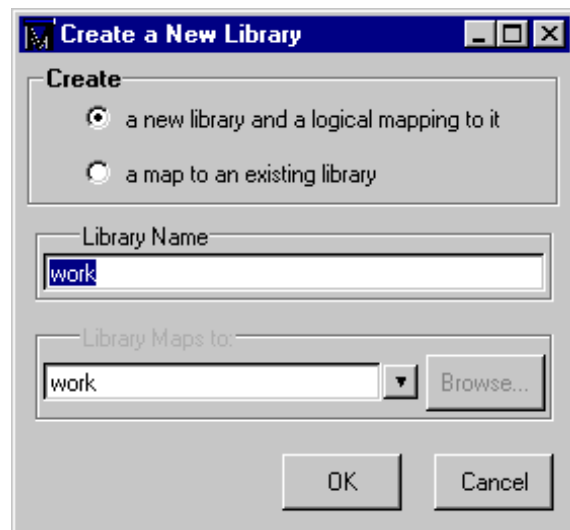
Select "Proceed to ModelSim" if the Welcome dialog appears.

- 3 Before you compile any HDL code, you'll need a design library to hold the compilation results. To create a new design library, make this menu selection in the Main window: **Design > Create a New Library**.

Make sure **Create: a new library and a logical mapping to it** is selected. Type "work" in the Library Name field and then select **OK**.

This creates a subdirectory named *work* - your design library - within the current directory. *ModelSim* saves a special file named *_info* in the subdirectory.

```
(PROMPT: vlib work
vmap work work)
```



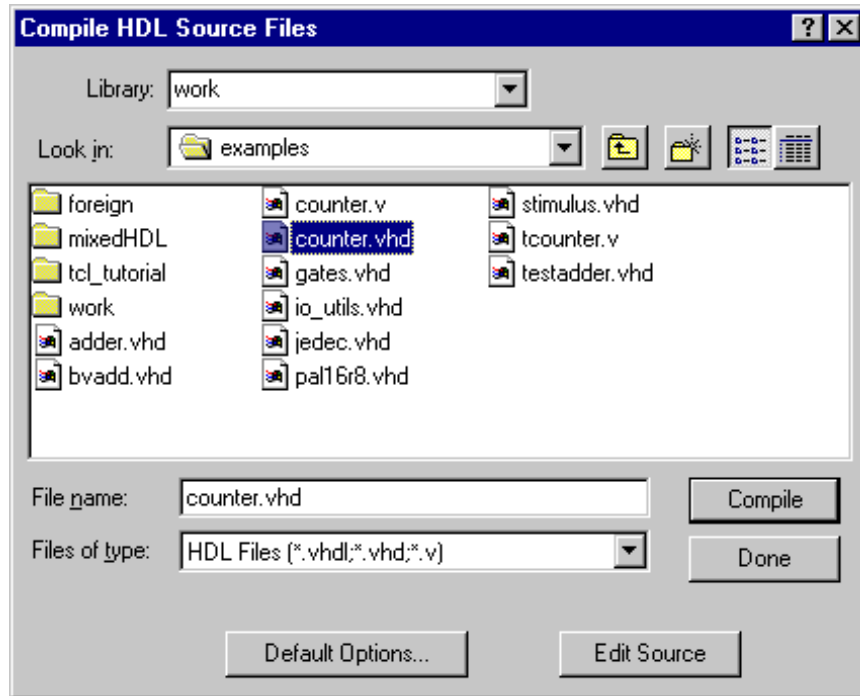
- ▶ **Note:** Do not create a Library directory using UNIX or Windows commands, because the *_info* file will not be created. Always use the Design menu or the **vlib** command from either the *ModelSim* or UNIX/DOS prompt.)

- 4 Compile the file *counter.vhd* into the new library by selecting the **Compile** button on the toolbar:



(PROMPT: vcom counter.vhd)

This opens the Compile HDL Source Files dialog box. (You won't see this dialog box if you invoke vcom from the command line.)



Complete the compilation by selecting *counter.vhd* from the file list and clicking **Compile**. Select **Done** when you are finished.

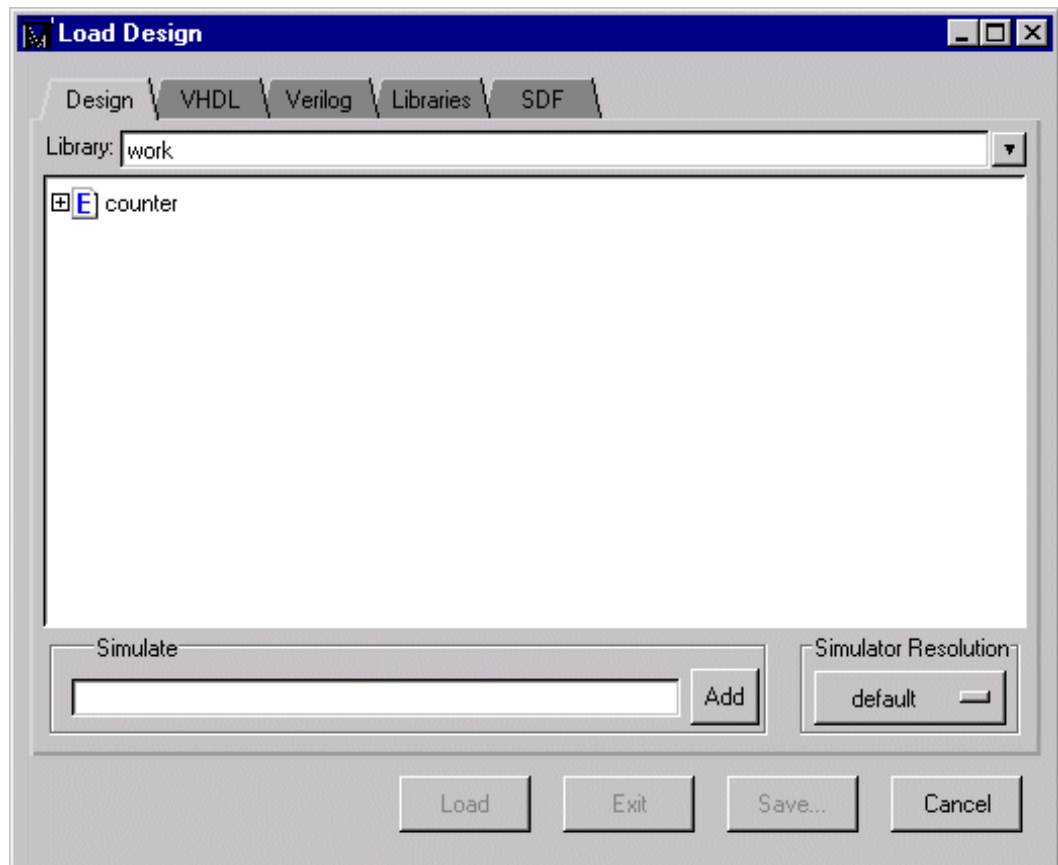
You can compile multiple files in one session from the file list. Individually select and Compile the files in the order required by your design.

- 5 Now let's load the design unit. Select the **Load Design** button from the toolbar:



(PROMPT: vsim counter)

The Load Design dialog box comes up, as shown below (you won't see this dialog box if you invoke **vsim** with *counter* from the command line).



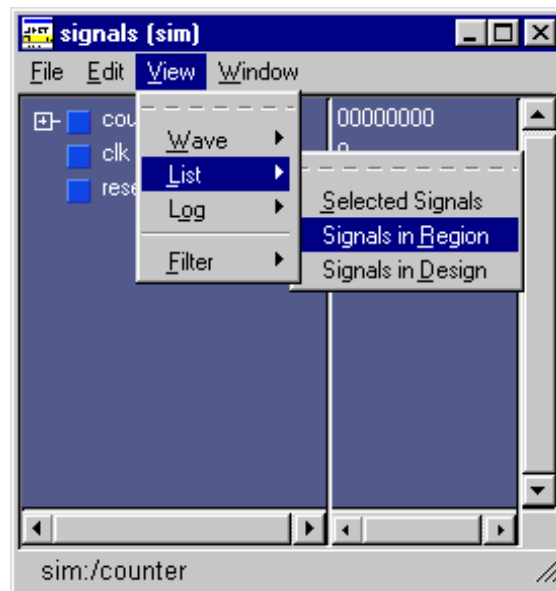
The Load Design dialog box lets you select the library and top-level design unit to simulate. You can also select the resolution limit for this simulation. By default, the following will appear for this simulation run:

- Simulator Resolution: default (the default is 1 ns)
- Library: work
- Design Unit: counter

If the Design Unit is an entity (like **counter** in this design), you can click on the plus-box prefix to view any associated architectures.



- 6 Select the entity **counter** and choose **Load** to accept these settings.
- 7 Next, select **View > All** from the Main window menu to open all ModelSim windows.
(PROMPT: view *)
For descriptions of the windows, consult the *ModelSim User's Manual*.
- 8 From the Signals window menu, select **View > List > Signals in Region**. This command displays the top-level signals in the List window.
(PROMPT: add list /counter/*)



- 9 Next add top-level signals to the Wave window by selecting **View > Wave > Signals in Region** from the Signals window menu.
(PROMPT: add wave /counter/*)

Running the simulation

We will start the simulation by applying stimulus to the clock input.

- 1 Click in the Main window and enter the following command at the VSIM prompt:

```
force clk 1 50, 0 100 -repeat 100
```

(MENU: Signals > Edit > Clock)

ModelSim interprets this **force** command as follows:

- force clk to the value 1 at 50 ns after the current time
 - then to 0 at 100 ns after the current time
 - repeat this cycle every 100 ns
- 2 Now you will exercise two different **Run** functions from the toolbar buttons on either the Main or Wave window. (The **Run** functions are identical in the Main and Wave windows.) Select the **Run** button first. When the run is complete, select **Run All**.



Run. This causes the simulation to run and then stop after 100 ns.

(PROMPT: run 100) (MENU: Run > Run 100ns)



Run -All. This causes the simulator to run forever. To stop the run, go on to the next step.

(PROMPT: run -all) (MENU: Run > Run -All)

- 3 Select the **Break** button on either the **Main** or **Wave** toolbar to interrupt the run. The simulator will stop running as soon as it gets to an acceptable stopping point.

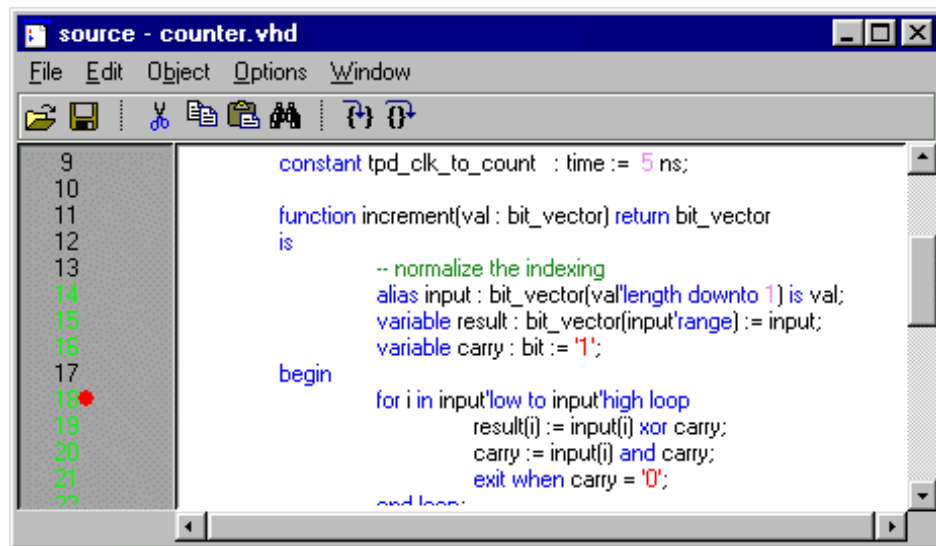


The arrow in the Source window points to the next HDL statement to be executed. (If the simulator is not evaluating a process at the time the Break occurs, no arrow will be displayed in the Source window.)

Next, you will set a breakpoint in the function on line 18.

- 4 Move the pointer to the Source window. Scroll the window vertically until line 18 is visible. Click on or near line number 18 to set the breakpoint. You should see a red dot next to the line number where the breakpoint is set. The breakpoint can be toggled between enabled and disabled by clicking it. When a breakpoint is disabled, the circle appears open. To delete the breakpoint, click the line number with your right mouse button and select Remove Breakpoint 18.

(PROMPT: bp counter.vhd 18)



- **Note:** Breakpoints can be set only on executable lines — denoted by green line numbers.

- 5 Select the **Continue Run** button to resume the run that you interrupted. ModelSim will hit the breakpoint, as shown by an arrow in the Source window and by a Break message in the Main window.



(PROMPT: run -continue) (MENU: Run > Continue)

- 6 Click the **Step** button to single-step through the simulation. Notice that the values change in the Variables window. You can keep clicking **Step** if you wish.



(PROMPT: run -step) (PROMPT: step)

- 7 When you're done, quit the simulator by entering the command:

```
quit -force
```

This command exits ModelSim without asking for confirmation.

Lesson 3 - Basic Verilog simulation

The goals for this lesson are:

- Compile a Verilog design
- List signals in the design
- Examine the hierarchy of the design
- Simulate the design
- Change list attributes
- Set a breakpoint

The project feature covered in Lesson 1 executes several actions automatically such as creating and mapping work libraries. In this lesson we will go through the whole process so you get a feel for how ModelSim really works.

Preparing the simulation

If you've completed any previous VHDL lesson, you'll notice that Verilog and VHDL simulation processes are almost identical.

- 1 Create and change to a new directory to make it the current directory.

You can make the directory current by invoking *ModelSim* from the new directory or by using the **File > Change Directory** command from the *ModelSim* Main window.

- 2 Copy the Verilog files (files with ".v" extension) from the `\<install_dir>\modeltech\examples` directory into the current directory.

Before you can compile a Verilog design, you need to create a design library in the new directory. If you are familiar only with interpreted Verilog simulators such as Cadence Verilog-XL, this will be a new idea for you. Since *ModelSim* is a compiled Verilog simulator, it requires a target design library for the compilation. *ModelSim* can compile both VHDL and Verilog code into the same library if desired.

- 3 Invoke *ModelSim*:

for UNIX at the shell prompt:

```
vsim
```

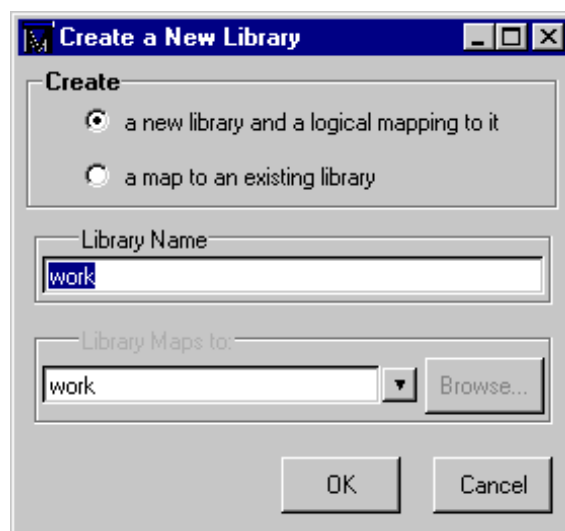
for Windows - your option - from a Windows shortcut icon, from the Start menu, or from a DOS prompt:

```
modelsim.exe
```

Select "Proceed to ModelSim" if the Welcome dialog appears.

- 4 Before you compile a source file, you'll need a design library to hold the compilation results. To create a new design library, select **Design > Create a New Library** in the Main window. (PROMPT: vlib work)

In the Create a New Library dialog box, select **Create: a new library and a logical mapping to it**. Type "work" in the **Library Name** field, and then select **OK**. This creates a subdirectory named *work* - your design library - within the current directory. This subdirectory contains a special file named *_info*.



- ▶ **Note:** Do not use UNIX/DOS commands to create a design library. Always use the Main Design menu or the **vlib** command.

Next, you'll compile the Verilog design.

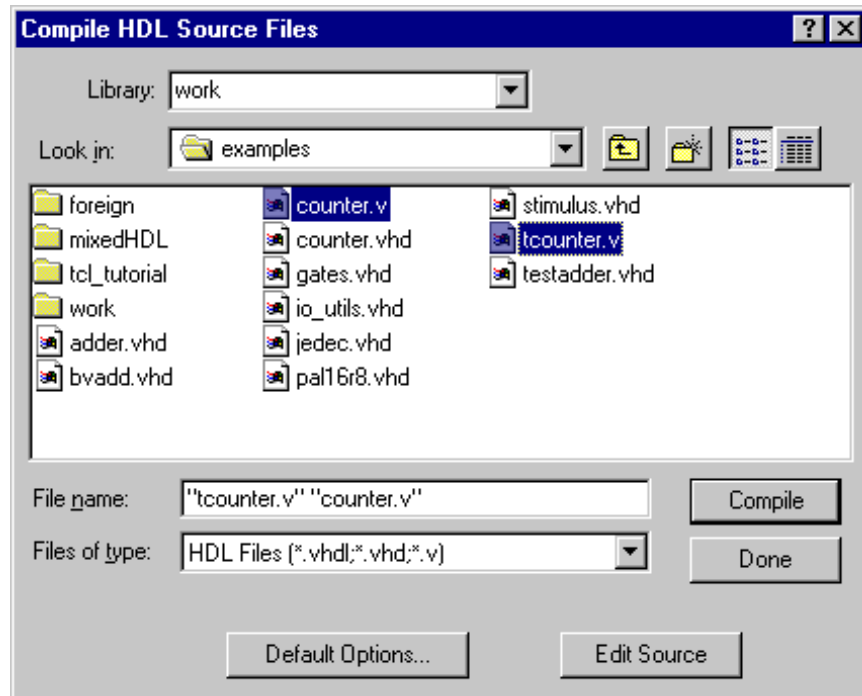
The example design consists of two Verilog source files, each containing a unique module. The file *counter.v* contains a module called **counter**, which implements a simple 8-bit binary up-counter. The other file, *tcounter.v*, is a testbench module (**test_counter**) used to verify **counter**. Under simulation you will see that these two files are configured hierarchically with a single instance (instance name **dut**) of module **counter** instantiated by the testbench. You'll get a chance to look at the structure of this code later. For now, you need to compile both files into the **work** design library.

- 5 Compile the *counter.v*, and *tcounter.v* files into the **work** library by selecting the **Compile** button on the toolbar:



(PROMPT: vlog counter.v tcounter.v)

This opens the Compile HDL Source Files dialog box.



Complete the compilation by selecting both files. **Control+click** (left mouse button) on *counter.v*, then *tcounter.v* from the file list and choose **Compile**, then **Done**.

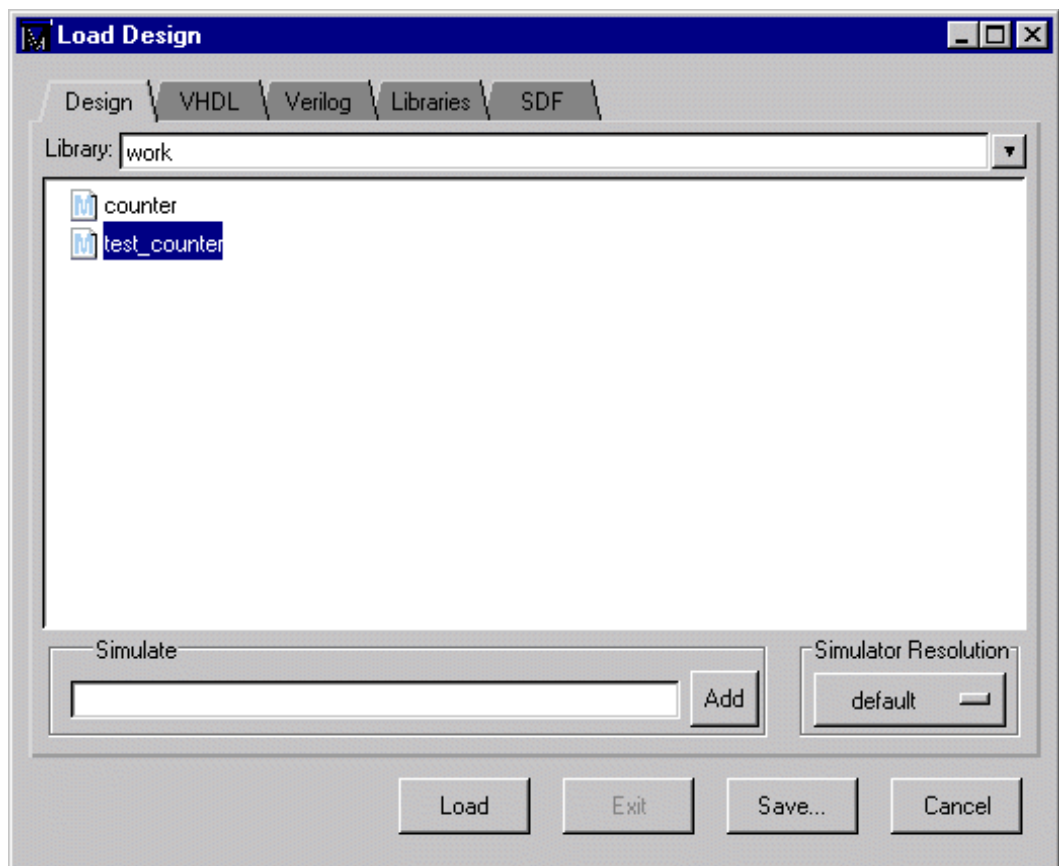
- ▶ **Note:** The order in which you compile the two Verilog modules is not important (other than the source-code dependencies created by compiler directives). This may again seem strange to Verilog-XL users who understand the possible problems of interface checking between design units, or compiler directive inheritance. ModelSim defers such checks until the design is loaded. So it doesn't matter here if you choose to compile *counter.v* before or after *tcounter.v*.

- 6 Start the simulator by selecting the **Load Design** button from the toolbar:



(PROMPT: vsim test_counter)

The Load Design dialog box comes up, as shown below.



The Load Design dialog box allows you to select a design unit to simulate from the specified library. You can also select the resolution limit for the simulation. The default library is **work** and the default resolution is 1 ns.

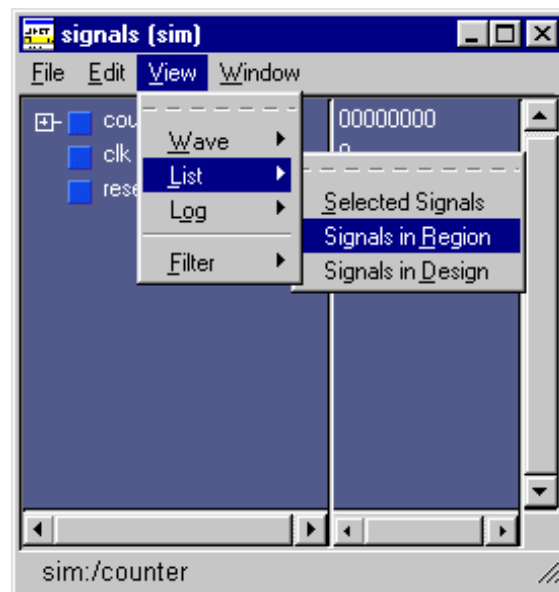
- 7 Select **test_counter** and click **Load** to accept these settings.
- 8 Bring up the Signals, List and Wave windows by entering the following command at the VSIM prompt within the Main window:

```
view signals list wave
```

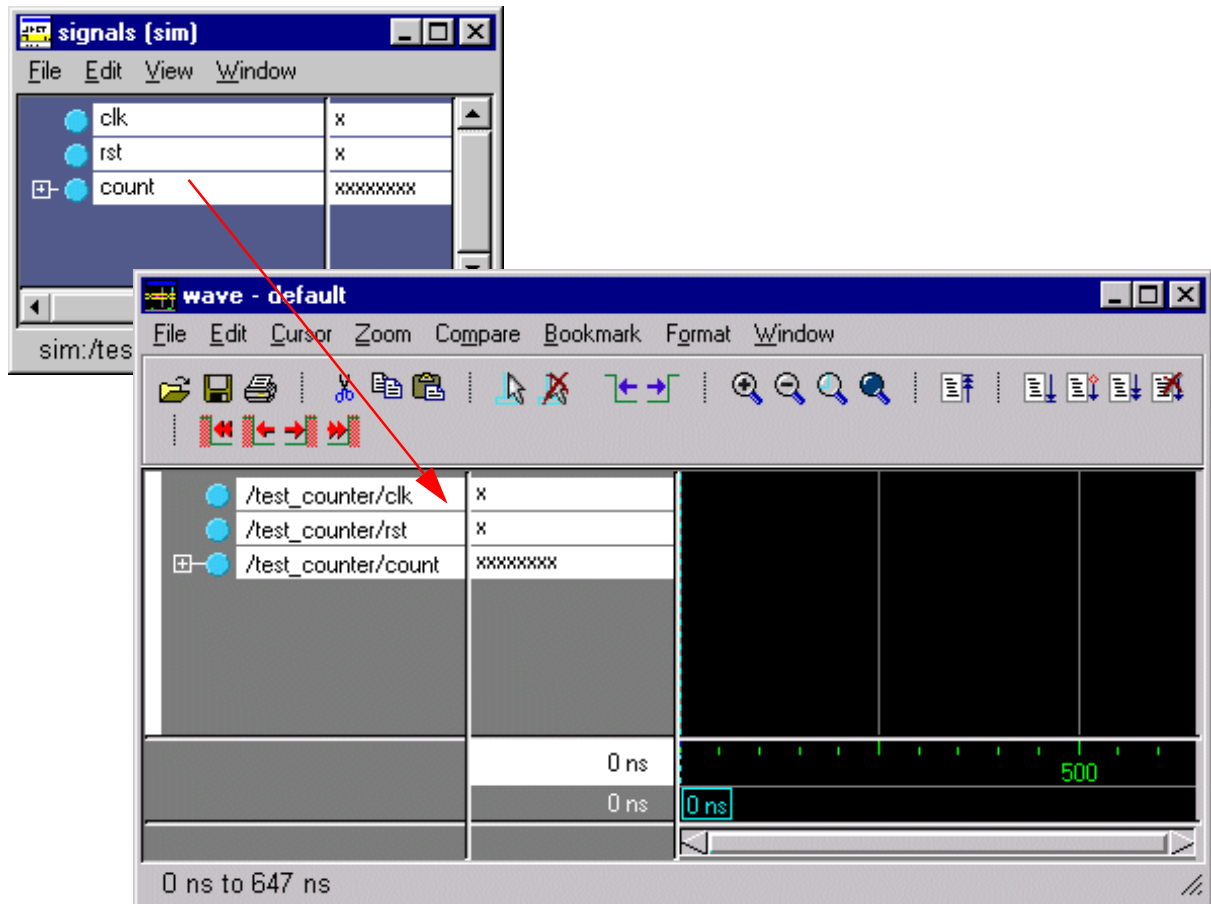
(Main MENU: View > <window name>)

- 9 To list the top-level signals, move the pointer to the Signals window and select **View > List > Signals in Region**.

(PROMPT: add list /test_counter/*)



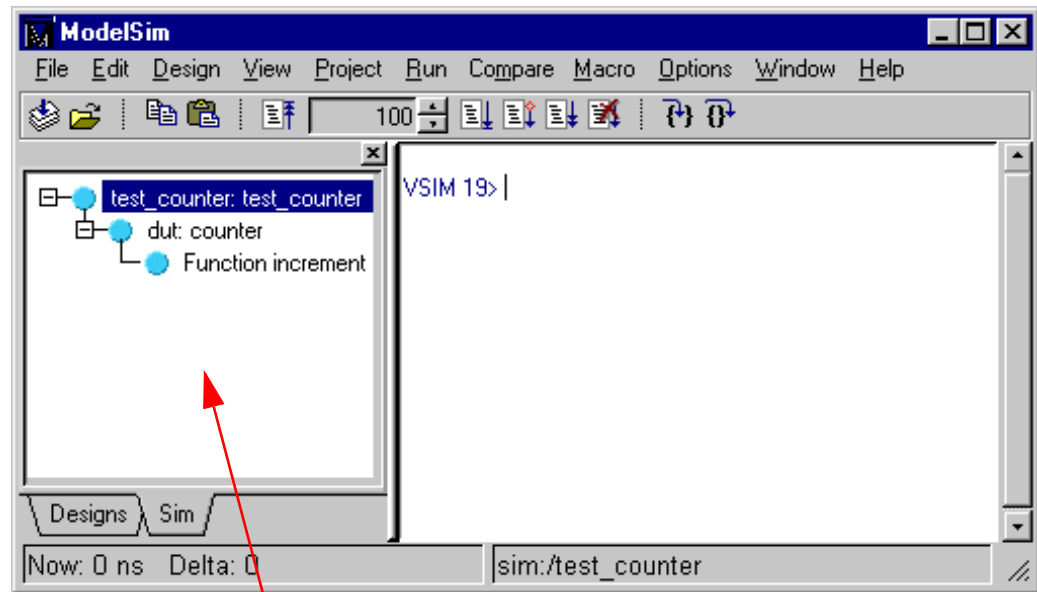
- 10 Now let's add signals to the Wave window with ModelSim's drag and drop feature. In the Signals window, select **Edit > Select All** to select the three signals. Drag the signals to either the pathname or the values pane of the Wave window.



HDL items can also be copied from one window to another (or within the Wave and List windows) with the **Edit > Copy** and **Edit > Paste** menu selections. You can also delete selected items with the **Edit > Delete** selection.

- 11 Next open the Source window. Select **View > Source** from the Main window. (PROMPT: view source)

- 12 You may have noticed when you loaded the design in Step 6 that a new pane appeared in the workspace area of the Main window.



Structure pane

The Structure pane shows the hierarchical structure of the design. By default, only the top level of the hierarchy is expanded. You can navigate within the hierarchy by clicking on any line with a "+" (expand) or "-" (contract) symbol. The same navigation technique works anywhere you find these symbols within ModelSim.

By clicking the "+" next to **dut: counter** you can see all three hierarchical levels: **test_counter**, **counter** and a function called **increment**. (If **test_counter** is not displayed you simulated **counter** instead of **test_counter**.)

- 13 Click on **Function increment** and notice how other ModelSim windows are automatically updated as appropriate.

Specifically, the Source window displays the Verilog code at the hierarchical level you selected in the Structure window. The source-file name is also displayed in the Source window title bar.

Using the Structure pane in this way is analogous to scoping commands in interpreted Verilogs.

For now, make sure the **test_counter** module is showing in the Source window by clicking on the top line in the Structure pane.

Running the simulation

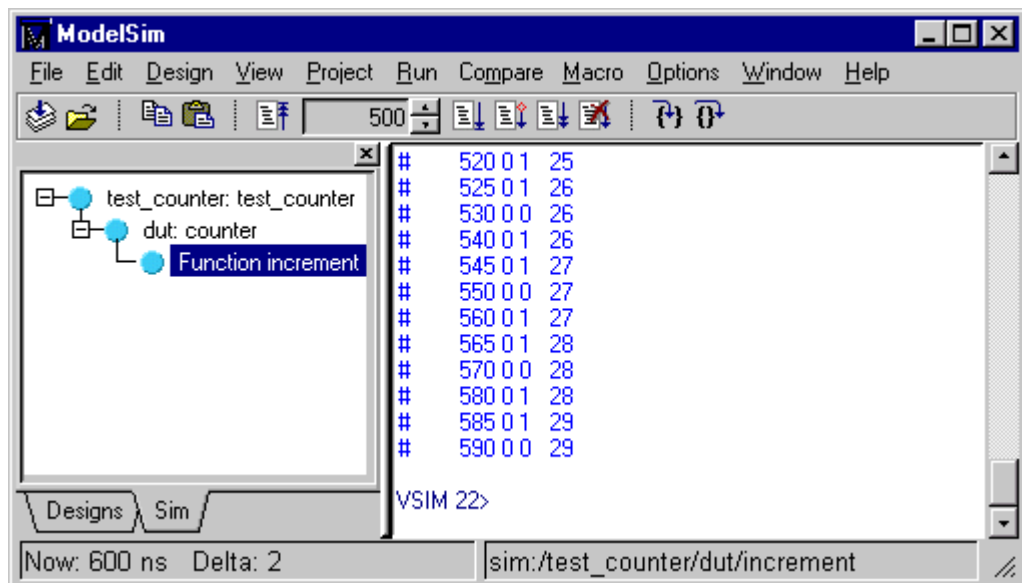
Now you will exercise different Run functions from the toolbar.

- 1 Select the **Run** button on the Main window toolbar. This causes the simulation to run and then stop after 100 ns (the default simulation length).



(PROMPT: run) (MENU: Run > Run 100 ns)

- 2 Next change the run length to 500 on the **Run Length** selector and select the **Run** button again.



Now the simulation has run for a total of 600ns (the default 100ns plus the 500 you just asked for). The status bar at the bottom of the Main window displays this information.

- 3 The last command you executed (**run 500**) caused the simulation to advance for 500ns. You can also advance simulation to a specific time. Type:

```
run @ 3000
```

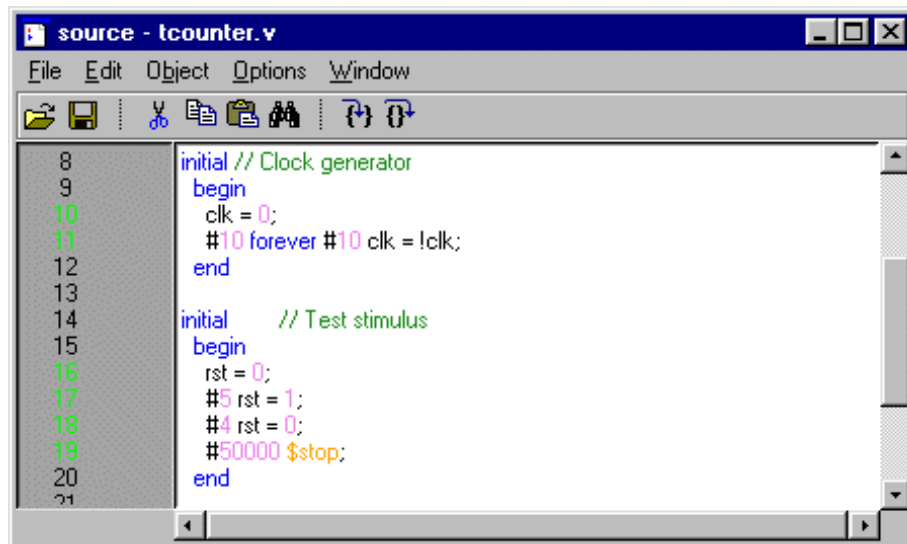
This advances the simulation to time 3000ns. Note that the simulation actually ran for an additional 2400ns (3000 - 600).

- 4 Now select the **Run All** button from the Main window toolbar. This causes the simulator to run forever.



(PROMPT: run -all) (Main MENU: Run > Run -All)

- 5 Select the **Break** button to interrupt the run.

A screenshot of the 'source - tcounter.v' window in ModelSim SE. The window has a menu bar with 'File', 'Edit', 'Object', 'Options', and 'Window'. Below the menu bar is a toolbar with icons for file operations and simulation control. The main area contains Verilog code with line numbers 8 through 21 on the left. The code is color-coded: comments are green, keywords are blue, and values are black. The code defines a clock generator and a test stimulus.

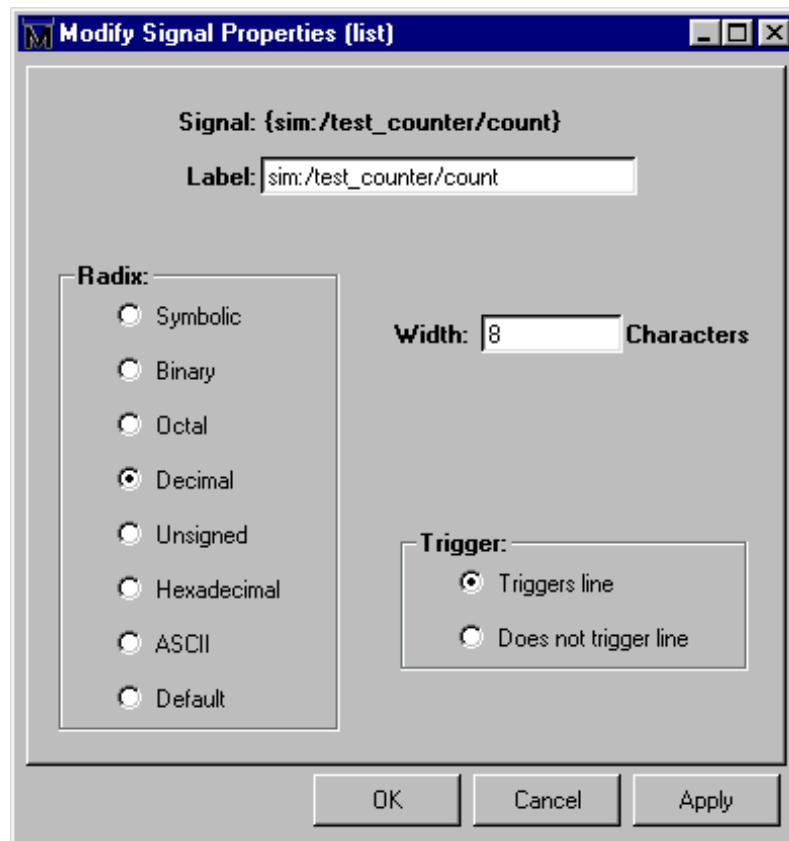
```
8 initial // Clock generator
9 begin
10 clk = 0;
11 #10 forever #10 clk = !clk;
12 end
13
14 initial // Test stimulus
15 begin
16 rst = 0;
17 #5 rst = 1;
18 #4 rst = 0;
19 #50000 $stop;
20 end
21
```

Your Source window won't look exactly like the illustration above because your simulation very likely stopped at a different point.

Debugging the simulation

Next we'll take a brief look at some interactive debug features of the ModelSim environment. To start with, let's see what we can do about the way the List window presents its data.

- 1 In the List window select `/test_counter/count`. From the List window menu bar select **Prop > Signal Props**. The Modify Signal Properties (list) dialog box is opened.

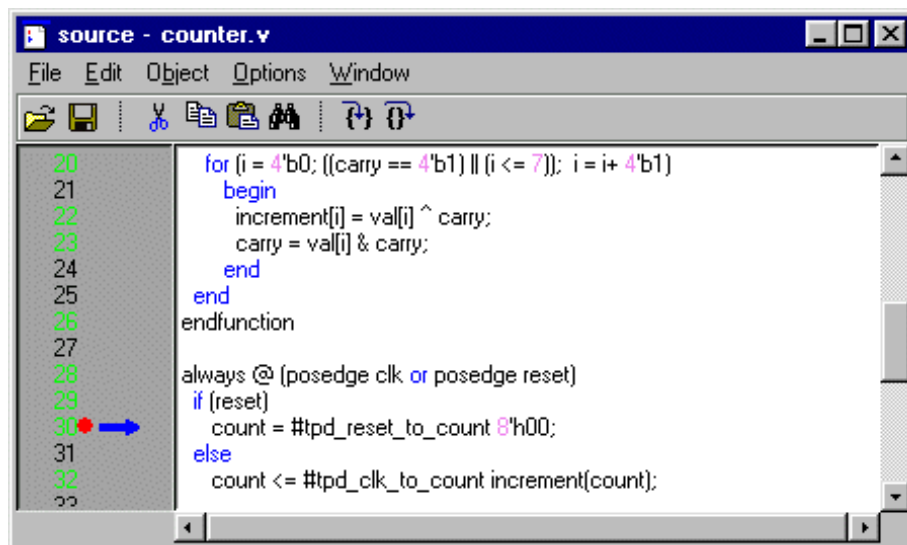


Select a display radix of **Decimal** for the signal **count**. Click **OK**. This causes the List window output to change; the count signal is now listed in decimal rather than the default binary.

- Now let's set a breakpoint at line 30 in the `counter.v` file (which contains a call to the Verilog function `increment`). To do this, select **dut: counter** in the Structure pane of the Workspace. Move the cursor to the Source window and scroll the window to display line 30. Click on or near line number 30 to set a breakpoint. You should see a red dot next to the line number where the breakpoint is set.

The breakpoint can be toggled between enabled and disabled by clicking it. When a breakpoint is disabled, the circle appears open. To delete the breakpoint, click the line number with your right mouse button and select `Remove Breakpoint`.

- **Note:** Breakpoints can be set only on executable lines — denoted by green line numbers.



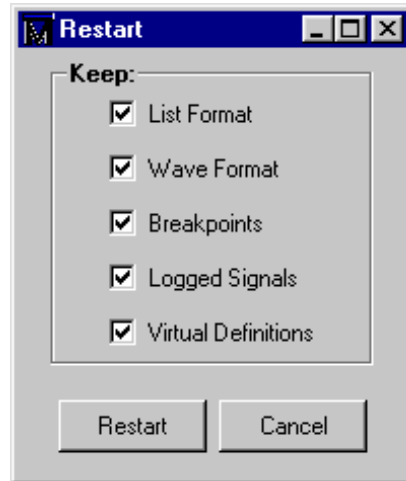
```
20   for (i = 4'b0; ((carry == 4'b1) || (i <= 7)); i = i + 4'b1)
21     begin
22       increment[i] = val[i] ^ carry;
23       carry = val[i] & carry;
24     end
25   end
26 endfunction
27
28 always @ (posedge clk or posedge reset)
29   if (reset)
30     count = #tpd_reset_to_count 8'h00;
31   else
32     count <= #tpd_clk_to_count increment(count);
33
```

- Select the **Restart** button to reload the design elements and reset the simulation time to zero.



(Main MENU: File > Restart) (PROMPT: restart)

Make sure all items in the Restart dialog box are selected, then click **Restart**.



- ▶ **Note:** The Verilog code in this example has a "stop" statement on line 19. If you resume the execution of the simulation without restarting first, you will stop at that line.

- 4 Select the **Run -all** button from the Main window toolbar to resume execution of the simulation.



(PROMPT: run -all) (Main MENU: Run > Run -All)

When the simulation hits the breakpoint, it stops running, highlights the line with an arrow in the Source window, and issues a Break message in the Main window.

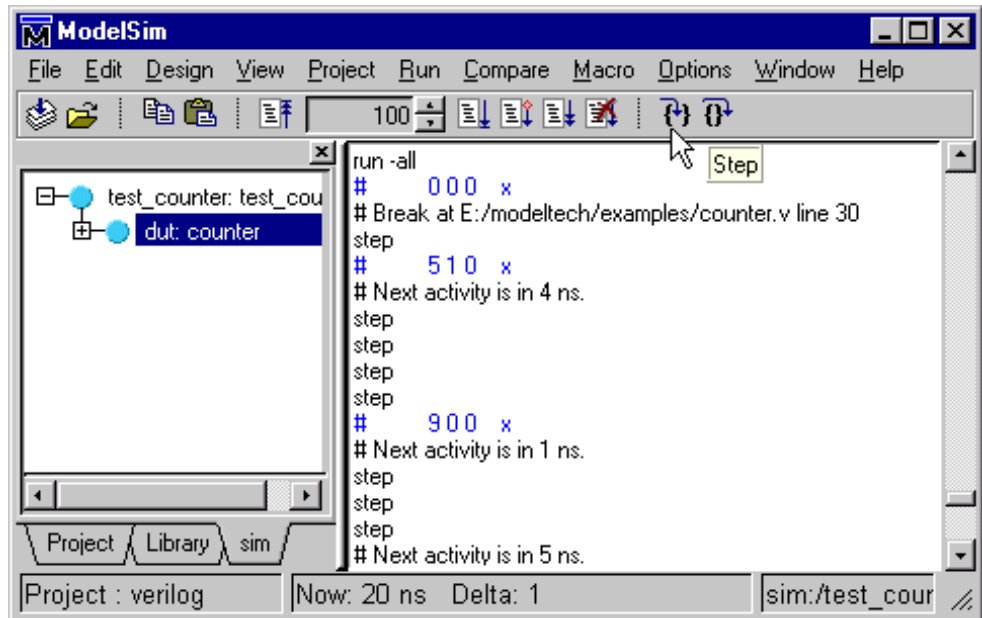
- 5 Typically when a breakpoint is reached you will be interested in one or more signal values. You have several options for checking values.

You can look at the values shown in the Signals window; you can move your mouse pointer over the *count* variable in the Source window and press the right mouse button; or you can use the **examine** command:

```
examine count
```

As a result of your command the count is output to the Main window.

- Let's move through the Verilog source functions with ModelSim's Step command. Click **Step** on the toolbar.



The Step button on the toolbar single-steps the debugger.

- Experiment by yourself for awhile. Set and clear breakpoints and use the Step and Step Over commands until you feel comfortable with their operation. When you're done, quit the simulator by entering the command:

```
quit -force
```


Lesson 4 - Mixed VHDL/Verilog simulation

The goals for this lesson are:

- Compile multiple VHDL and Verilog files
- Simulate a mixed VHDL and Verilog design
- List VHDL signals and Verilog nets and registers
- View the design in the Structure window
- View the HDL source code in the Source window

▶ **Note:** You must be using *ModelSim SE/PLUS* or *ModelSim SE/MIXED* to do this lesson.

Preparing the simulation

- 1 Start by creating a new directory for this exercise. Create the directory, then copy the VHDL and Verilog example files to the directory:

```
<install_dir>\modeltech\examples\mixedHDL\*.vhd
<install_dir>\modeltech\examples\mixedHDL\*.v
```

Make sure the new directory is the current directory. Do this by invoking *ModelSim* from the new directory or by using the **File > Change Directory** command from the *ModelSim* Main window.

- 2 Start *ModelSim* with one of the following:

for UNIX at the shell prompt:

```
vsim -gui
```

for Windows - your option - from a Windows shortcut icon, from the Start menu, or from a DOS prompt:

```
modelsim.exe
```

- ▶ **Note:** If you didn't add *ModelSim* to your search path during installation, you will have to include the full path when you type this command at a DOS prompt.

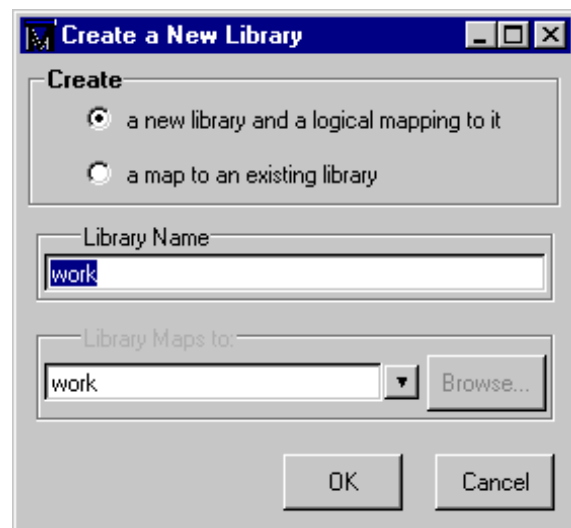
Select "Proceed to ModelSim" if the Welcome dialog appears.

- 3 Select **Design > Create a New Library** to create a new library to hold the mixed design.

(PROMPT: vlib work)

Type "work" in the **Library Name** field and then select **OK**.

This creates a subdirectory named *work* (your design library) within the current directory and a logical mapping to the library. The library contains a special file named *_info* that is created with the library.



- ▲ **Important:** Do not create library subdirectories using UNIX or Windows commands—always use the Design menu or the **vlib** command from either the *ModelSim* or UNIX/DOS prompt.

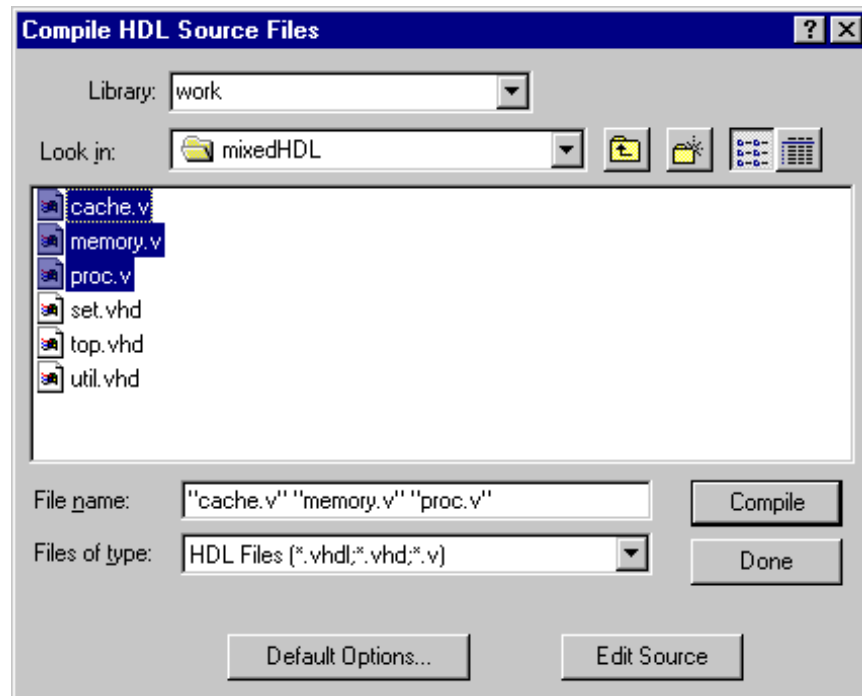
- 4 Compile the HDL files by selecting the **Compile** button on the toolbar:



(PROMPT: vlog cache.v memory.v proc.v)

(PROMPT: vcom util.vhd set.vhd top.vhd)

This opens the Compile HDL Source Files dialog box.



A group of Verilog files can be compiled in any order. Note, however, in a mixed VHDL/Verilog design the Verilog files must be compiled before the VHDL files.

Compile the source by double-clicking each of these Verilog files in the file list (this invokes the Verilog compiler, **vlog**):

- *cache.v*
- *memory.v*
- *proc.v*

- 5 Depending on the design, the compile order of VHDL files can be very specific. In the case of this lesson, the file *top.vhd* must be compiled last.

Stay in the Compile HDL Source Files dialog box and compile the VHDL files in this order (this invokes the VHDL compiler, **vcom**):

- *util.vhd*
- *set.vhd*
- *top.vhd*

- 6 Compiling is now complete, click **Done** to dismiss the dialog box.

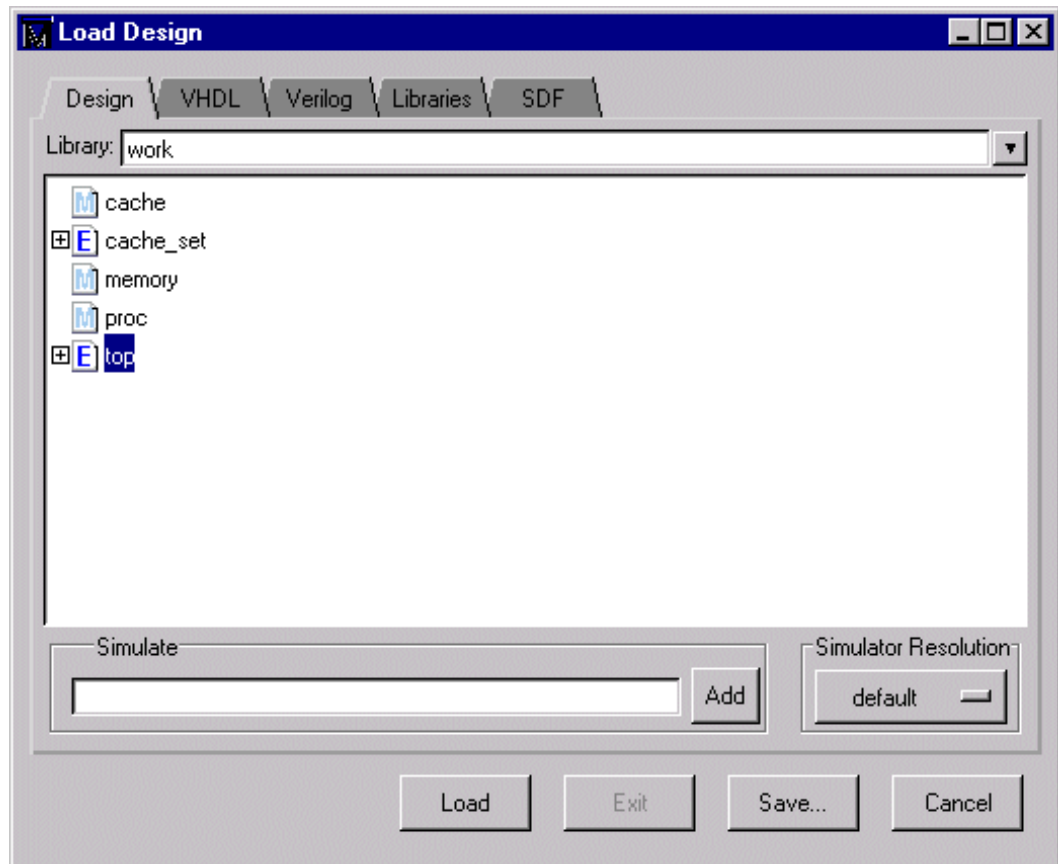
Running the simulation

- 1 Now it's time to simulate. Start the simulator by selecting the **Load Design** button from the Main toolbar:



(PROMPT: vsim top)

This returns the Load Design dialog box.



On the Design tab select the **top** entity and click **Load**.

- 2 From the Main menu select **View > All** to open all ModelSim windows.
(PROMPT: view *)

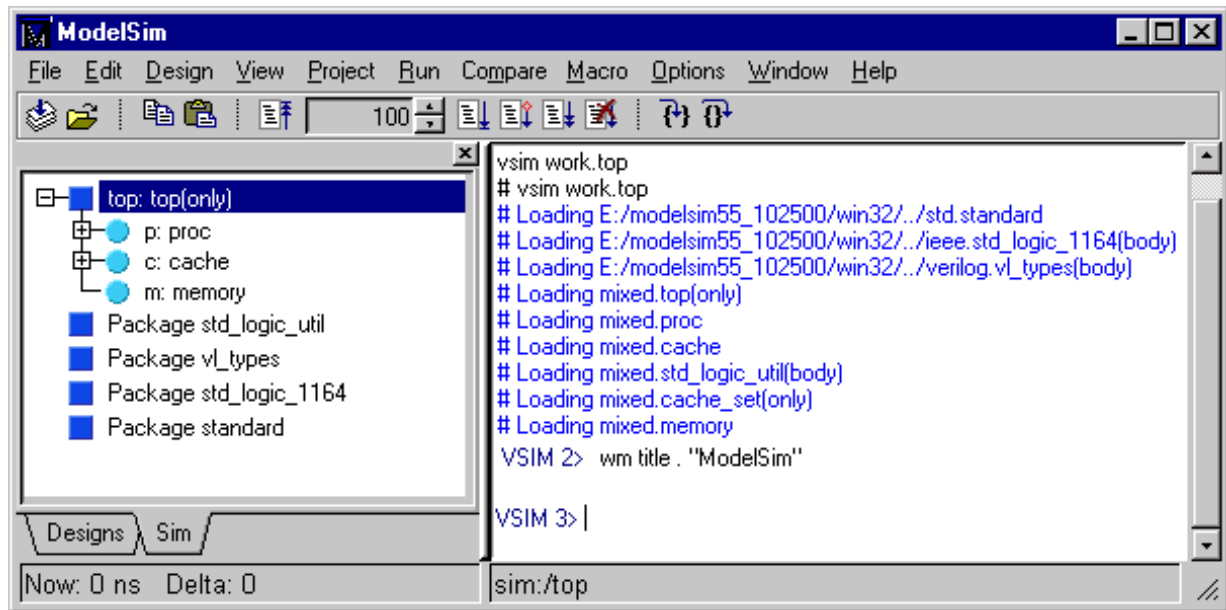
- 3 This time you will use the command line to add all of the HDL items in the region to the List and Wave windows:

```
add list *
add wave *
```

(Signals MENU: View > List > Signals in Region)

(Signals MENU: View > Wave > Signals in Region)

- 4 Take a look at the Structure pane in the workspace.



Notice the hierarchical mixture of VHDL and Verilog in the design. VHDL levels are indicated by a square “prefix”, while Verilog levels are indicated by a circle “prefix.” Try expanding (+) and contracting (-) the structure layers. You’ll find Verilog modules have been instantiated by VHDL architectures, and similar instantiations of VHDL items by Verilog.

Let’s take another look at the design.

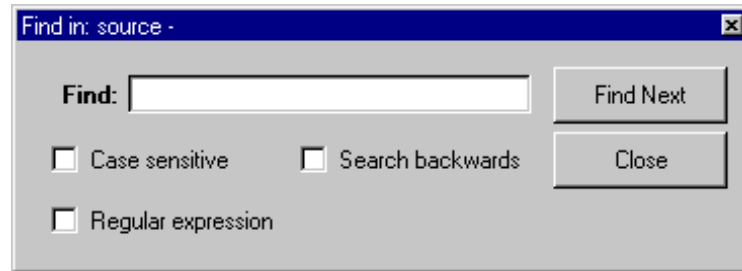
- 5 In the Structure pane, click on the Verilog module **c: cache**. The source code for the Verilog module is now shown in the Source window.

- 6 We'll use ModelSim's Find function to locate the declaration of `cache_set` within `cache.v`.

From the Source window menu select: **Edit > Find**:



The **Find in** dialog box is displayed.



In the **Find:** field, type `cache_set` and click **Find Next**. The `cache_set` instantiations are now displayed in the Source window. (Click **Close** to dismiss the **Find in:** dialog box.)

Note that `cache_set` is a VHDL entity instantiated within the Verilog file `cache.v`.

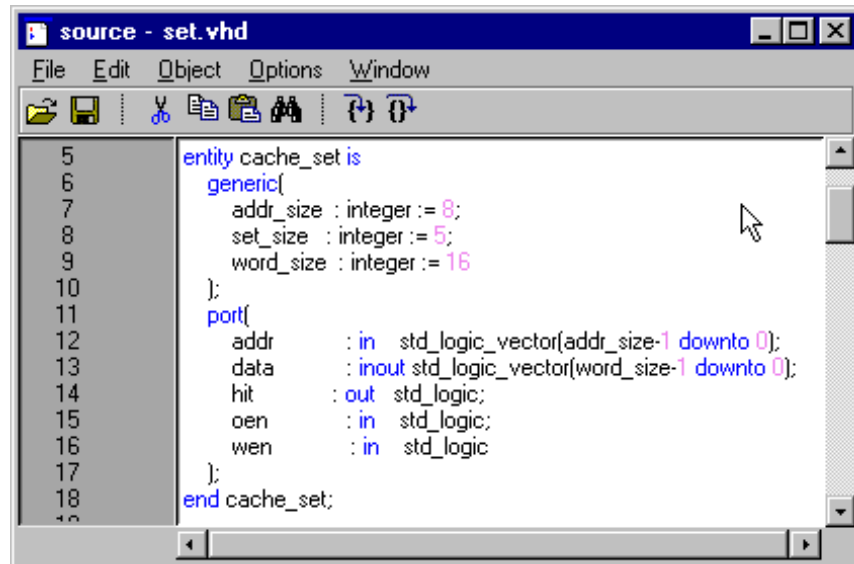
```

20  wire      #(5) srw = srw_r, sstrb = sstrb_r, prdy = prdy_r;
21
22  reg [3:0] oen, wen;
23  wire [3:0] hit;
24
25  /***** Cache sets *****/
26  cache_set s0(paddr, pdata, hit[0], oen[0], wen[0]);
27  cache_set s1(paddr, pdata, hit[1], oen[1], wen[1]);
28  cache_set s2(paddr, pdata, hit[2], oen[2], wen[2]);
29  cache_set s3(paddr, pdata, hit[3], oen[3], wen[3]);
30
31  initial begin
32      verbose = 1;
33      saddr_r = 0;
34      sdata_r = 'bz;

```

- 7 Now click on the line "**s0: cache_set(only)**" in the Structure window. If instance s0 is not currently visible, click on the + next to c:cache.

The Source window shows the VHDL code for the cache_set entity.



```

source - set.vhd
File Edit Object Options Window
entity cache_set is
generic(
  addr_size : integer := 8;
  set_size  : integer := 5;
  word_size : integer := 16
);
port(
  addr      : in  std_logic_vector(addr_size-1 downto 0);
  data      : inout std_logic_vector(word_size-1 downto 0);
  hit       : out std_logic;
  oen       : in  std_logic;
  wen       : in  std_logic
);
end cache_set;

```

Before you quit, try experimenting with some of the commands you've learned from Lesson 1. Note that in this design, "clk" is already driven, so you won't need to use the **force** command.

- 8 When you're ready to quit simulating, enter the command:

```
quit -force
```

Lesson 5 - Debugging a VHDL design

The goals for this lesson are:

- Show an example of a VHDL testbench - a VHDL architecture that instantiates the VHDL design units to be tested, provides simulation stimuli, and checks the results
- Map a logical library name to an actual library
- Change the default run length
- Recognize assertion messages in the command window
- Change the assertion break level
- Restart the simulation run using the **restart** command
- Examine composite types displayed in the Variables window
- Change the value of a variable
- Use a strobe to trigger lines in the List window
- Change the radix of signals displayed in the List window

Preparing the simulation

- 1 Create a new directory for this exercise and copy the following VHDL (.vhd) files from `\<install_dir>\modeltech\examples` to the new directory.
 - gates.vhd
 - adder.vhd
 - testadder.vhd

- 2 Make sure the new directory is the current directory. Do this by invoking *ModelSim* from the new directory or by using the **File > Change Directory** command from the *ModelSim* Main window.

- 3 Start *ModelSim* with one of the following:

for UNIX at the shell prompt:

```
vsim
```

for Windows - your option - from a Windows shortcut icon, from the Start menu, or from a DOS prompt:

```
modelsim.exe
```

Select "Proceed to ModelSim" if the Welcome dialog appears.

- 4 Enter the following command at the *ModelSim* prompt to create a new library:


```
vlib library_2
```

- 5 Compile the source files into the new library by entering this command at the *ModelSim* prompt:


```
vcom -work library_2 gates.vhd adder.vhd testadder.vhd
```

- 6 Now let's map the new library to the work library. To create a mapping you can edit the [Library] section of the *modelsim.ini* file, or you can create a logical library name with the **vmap** command:

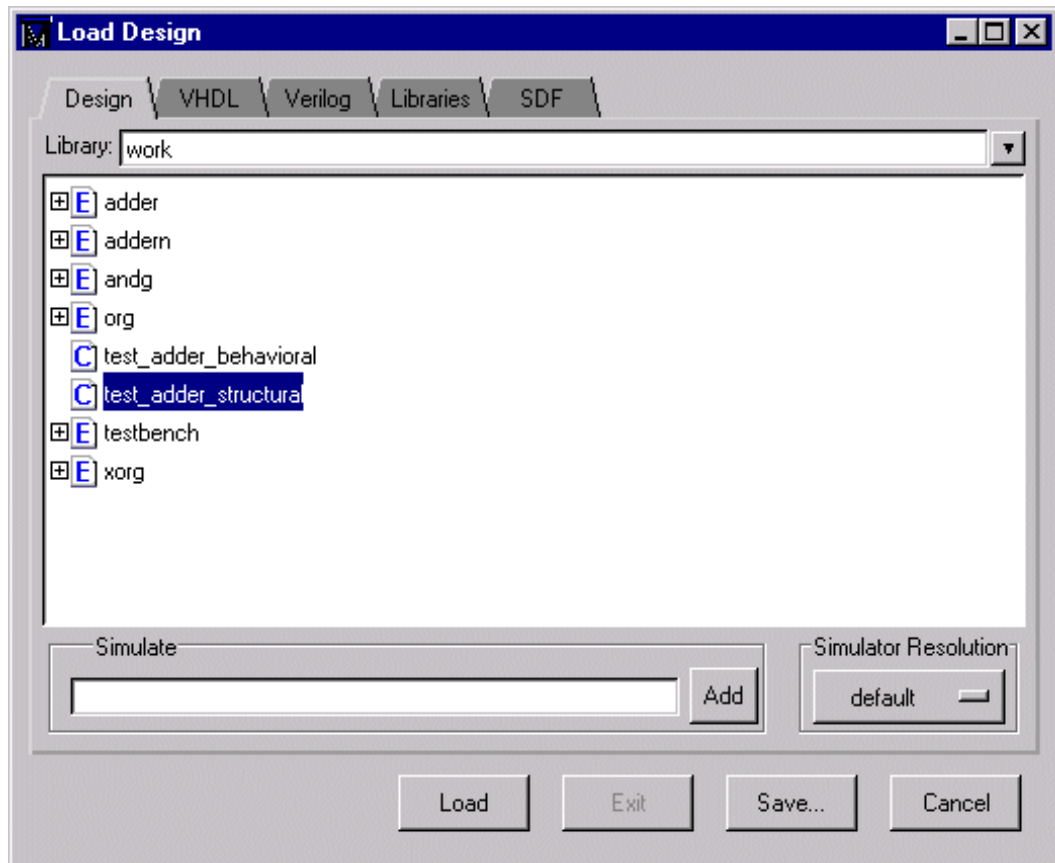

```
vmap work library_2
```

ModelSim modifies the *modelsim.ini* file for you.

- 7 Start the simulator by selecting **Design > Load Design** from the Main window, or by clicking the Load Design icon. The Load Design dialog box is displayed, as shown below.

- 8 Perform the following steps in the Load Design dialog box:
- Make sure that the simulator resolution is **default**.
 - Look in the Design Unit scroll box and select the configuration named **test_adder_structural**.
 - Click **Load** to accept the settings.

(PROMPT: vsim -t ns work.test_adder_structural)



- 9 To open all of the ModelSim windows, enter the following command in the Main window at the VSIM prompt:

```
view *
```

(Main MENU: View > All)

- 10 Drag and drop the top-level signals to the List window in the following manner: make sure the hierarchy is not expanded (no minus boxes), select all signals in the Signals window with **Edit > Select All**, then drag the selected signals to the List window.

(Signals MENU: View > List > Signals in Region) (PROMPT: add list *)

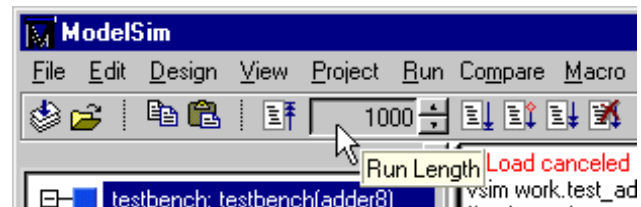
- 11 To add top-level signals to the Wave window, enter the command:

```
add wave *
```

(Signals MENU: View > Wave > Signals in Region) (DRAG&DROP)

- 12 Now change the default simulation run length to 1000 (ns) with the run length selector on the Main toolbar. Click on the field to edit the number to 1000 (notice how the arrows allow you to change the run length in increments).

(Main MENU: Options > Simulation > Defaults)



Running and debugging the simulation

- 1 Now you will run the simulator. Select the **Run** button on the Main window toolbar.



(PROMPT: run)

A message in the Main window will notify you that there was an assertion error.

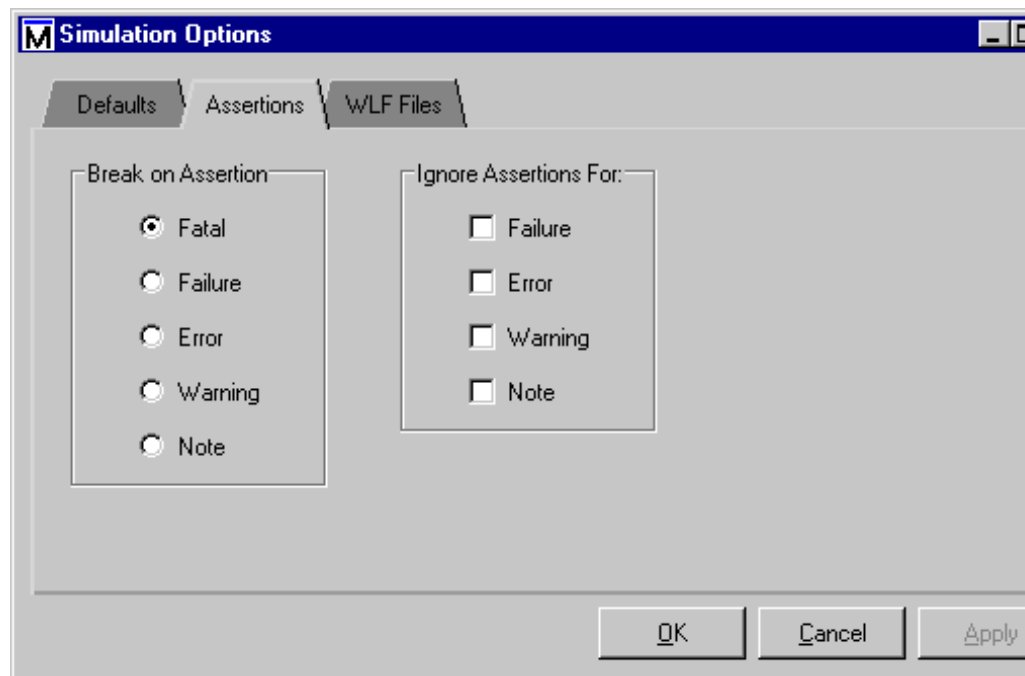
```
run
# ** Error: Sum is 00000111. Expected 00001000
#   Time: 600 ns Iteration: 0 Instance: /testbench
# ** Note: There were ERRORS in the test.
#   Time: 1 us Iteration: 0 Instance: /testbench

VSIM 10>
```

Now: 1 us Delta: 1 sim:/testbench

Let's find out what's wrong. Perform the following steps to track down the assertion message.

- 2 First, change the simulation assertion options. Select **Options > Simulation** from the Main window menu.

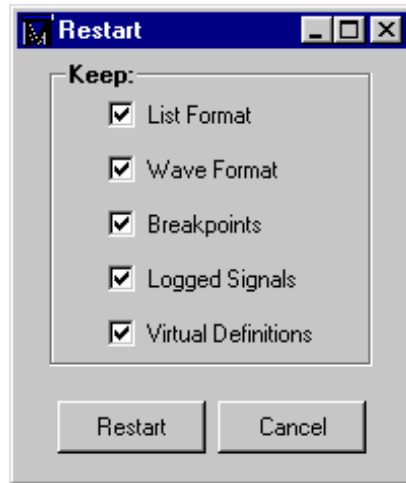


- 3 Select the **Assertions** page. Change the selection for **Break on Assertion** to **Error** and click **OK**. This will cause the simulator to stop at the HDL assertion statement.
- 4 To restart the simulation select the **Restart** button on the Main toolbar.



(Main MENU: File > Restart) (PROMPT: restart)

Make sure all items in the Restart dialog box are selected, then click **Restart**.

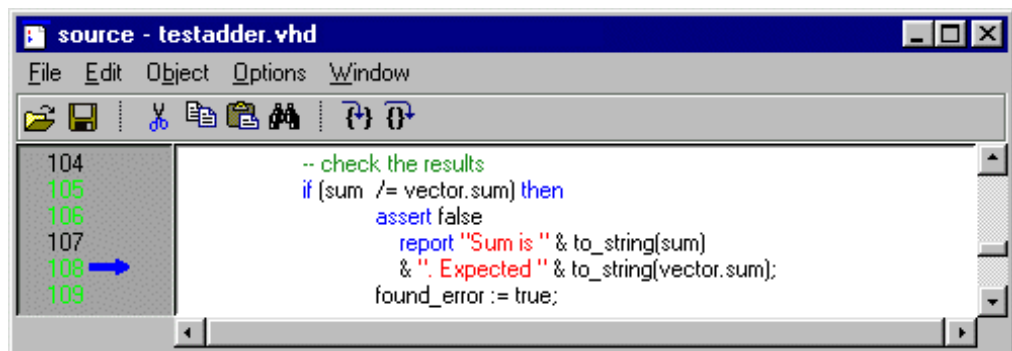


- 5 From the Main window toolbar select the **Run** button.

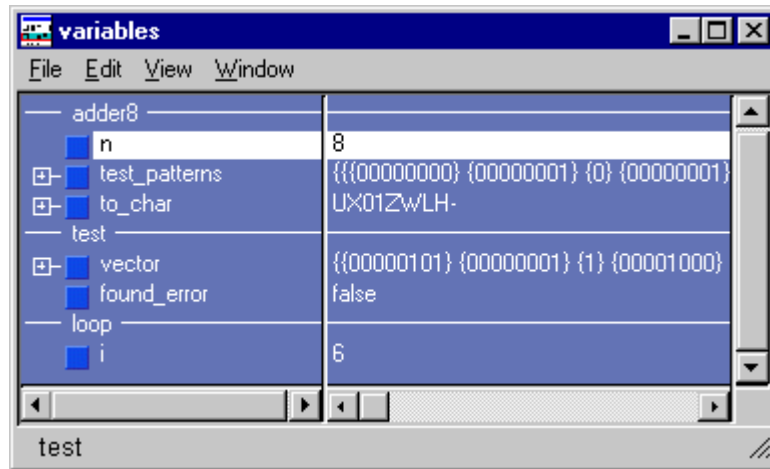


(Main MENU: Run > Run 1000 ns) (PROMPT: run)

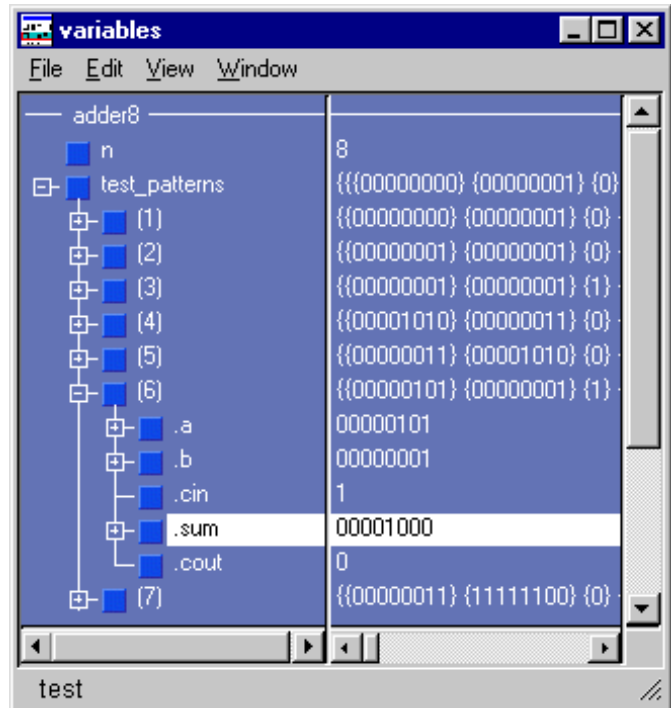
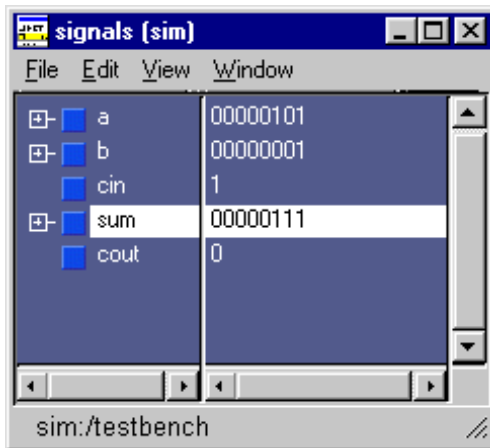
Notice that the arrow in the Source window is pointing to the assertion statement.



- 6 If you look at the Variables window now, you can see that $i = 6$. This indicates that the simulation stopped in the sixth iteration of the test pattern's loop.



- 7 Expand the variable named **test_patterns** by clicking the [+]. (You may need to resize the window for a better view.)
- 8 Also expand the sixth record in the array **test_patterns(6)**, by clicking the [+]. The Variables window should be similar to the one below.



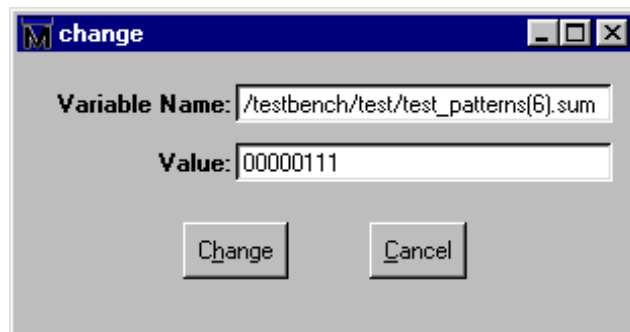
The assertion shows that the Signal **sum** does not equal the **sum** field in the Variables window. Note that the sum of the inputs **a**, **b**, and **cin** should be equal to the output **sum**. But there is an error in the test vectors. To correct this error, you need to restart the simulation and modify the initial value of the test vectors.

- 9 In the Main window, type:

```
restart -f
```

The **-f** option causes ModelSim to restart without popping up the confirmation dialog.

- 10 Update the Variables window by selecting the **testbench** process in the **test** Process window.
- 11 In the Variables window, expand **test_patterns** and **test_pattern(6)** again. Then highlight the **.sum** record by clicking on the variable name (not the box before the name) and then use the **Edit > Change** menu selection.



- 12 Select the last four bits (**1000**) in the value field by dragging the pointer across them. Then replace them with **0111**, and click **Change**. (Note that this is a temporary edit, you must use your text editor to permanently change the source code.)
- 13 Select the **Run** button from the Main window toolbar.



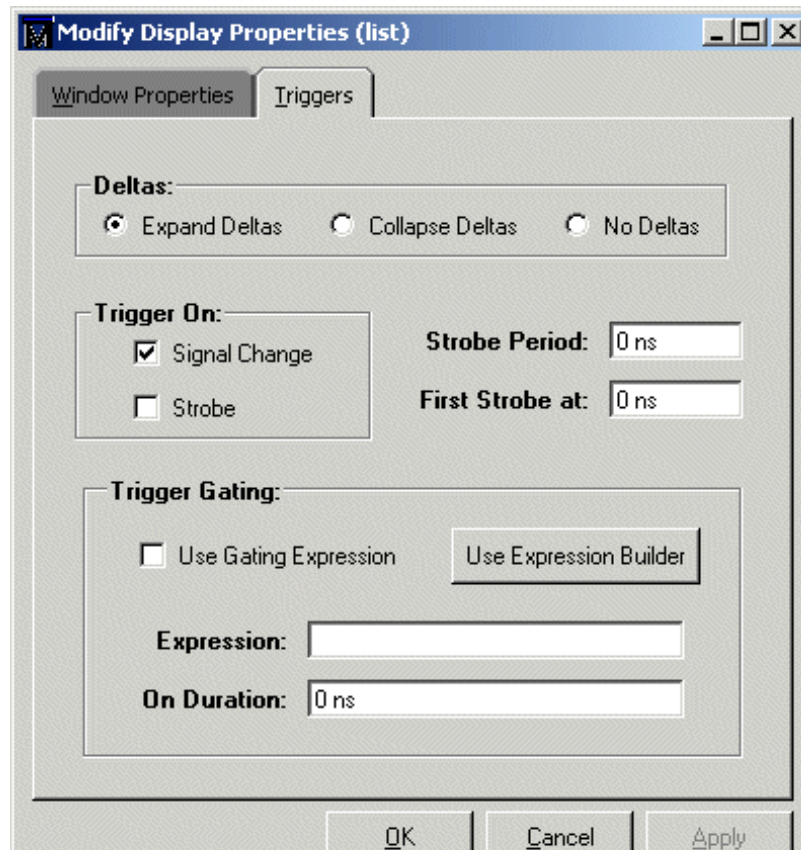
(Main MENU: Run > Run 1 us) (PROMPT: run)

At this point, the simulation will run without errors.

```
run
#** Note: Test completed with no errors.
# Time: 1 us Iteration: 0 Instance: /testbench
VSIM 14>
Now: 1 us Delta: 1 Env: /testbench
```

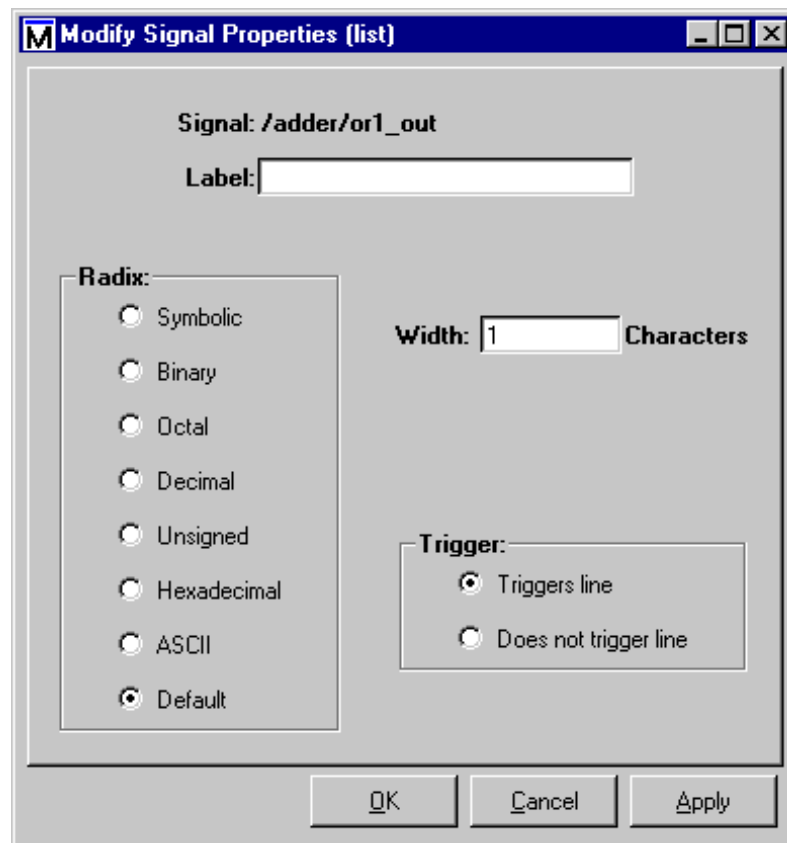
Changing new-line triggering

By default, a new line is displayed in the List window for each transition of a listed signal. The following steps will change the triggering so the values are listed every 100 ns.



- 1 In the List window, select **Prop > Display Props**.
- 2 Perform these steps on the **Triggers** page:
 - Deselect **Trigger On: Signals** to disable triggering on signals.
 - Select **Trigger On: Strobe** to enable the strobe.
 - Enter **100** in the **Strobe Period** field.
 - Enter **70** in the **First Strobe at** field.
 - Click **OK** to accept the settings.

- 3 Your last action will be to change the radix to decimal for signals a, b, and sum. Select **Prop > Signal Props**. This opens the Modify Signal Properties (list) dialog box.



- 4 In the List window select the signal you want to change, then make the property changes in the dialog box. Make the following property changes:
- Select signal **a**, then click **Decimal**, then click **Apply**.
 - Select signal **b**, then click **Decimal**, then **Apply**.
 - Select signal **sum**, then click **Decimal**, then **OK**.

This brings you to the end of this lesson, but feel free to experiment further with the menu system. When you are ready to end the simulation session, quit ModelSim by entering the following command at the VSIM prompt:

```
quit -force
```

Lesson 6 - Running a batch-mode simulation

The goals for this lesson are:

- Run a batch-mode VHDL simulation
- Execute a macro (DO) file
- View a saved simulation

Batch-mode allows you to execute several commands that are written in a text file. You create a text file with the list of commands you wish to run, and then specify that file when you start *ModelSim*. This is particularly useful when you need to run a simulation or a set of commands repeatedly.

▲ **Important:** Batch-mode simulations must be run from a DOS or UNIX prompt. In Windows, you get a DOS prompt by selecting **Start > Programs > Command Prompt**. Unless directed otherwise, enter all commands in this lesson at a DOS or UNIX prompt.

- 1 To set up for this lesson you'll need to create a new directory and make it the current directory. Copy this file into your new directory:

```
<install_dir>\modeltech\examples\counter.vhd
```

- 2 Create a new design library (Remember, enter these commands at a DOS or UNIX prompt):

```
vlib work
```

- 3 Map the library:

```
vmap work work
```

- 4 Then compile the source file:

```
vcom counter.vhd
```

- 5 You will use a macro file that provides stimulus for the counter. For your convenience, a macro file has been provided with ModelSim. You need to copy this macro file from the installation directory to the current directory:

```
<install_dir>\modeltech\examples\stim.do
```

- 6 Create a batch file using an editor; name it *yourfile*. With the editor, put the following on separate lines in the file:

```
add list -decimal *
do stim.do
write list counter.lst
```

and save to the current directory.

- 7 To run the batch-mode simulation, enter the following at the command prompt:

```
vsim -do yourfile -wlf saved.wlf counter
```

This is what you just did in Step 7:

- invoked the VSIM simulator on a design unit called "counter"
- instructed the simulator to save the simulation results in a log file named *saved.wlf* by using the **-wlf** switch
- used the contents of *yourfile* to specify that values are to be listed in decimal, to execute a stimulus file called *stim.do*, and to write the results to a file named *counter.lst*, the default for a design named counter

- 8 Since you saved the simulation results in *saved.wlf*, you can view the simulation results by starting up VSIM with its **-view** switch:

```
vsim -view saved.wlf
```

- 9 Open these windows with the **View** menu in the Main window, or the equivalent command at the *ModelSim* prompt:

```
view signals list wave
```

- ▶ **Note:** If you open the Process or Variables windows they will be empty. You are looking at a saved simulation, not examining one interactively; the logfile saved in *saved.wlf* was used to reconstruct the current windows.

- 10 Now that you have the windows open, put the signals in them:

```
add wave *  
add list *
```

- 11 Use the available windows to experiment with the saved simulation results and quit when you are ready:

```
quit -f
```

For additional information on the batch and command line modes, please refer to the *ModelSim User's Manual*.

Lesson 7 - Executing commands at startup

The goals for this lesson are:

- Specify the design unit to be simulated on the command line
- Edit the *modelsim.ini* file
- Execute commands at startup with a DO file

▲ **Important:** Start this lesson from either the UNIX or DOS prompt in the same directory in which you completed *Chapter Lesson 6 - Running a batch-mode simulation*.

- 1 For this lesson, you will use a macro (DO) file that provides startup information. For convenience, a startup file has been provided with the ModelSim program. You need to copy this DO file from the installation directory to your current directory:

```
<install_dir>\modeltech\examples\startup.do
```

- 2 Next, you will edit the modelsim.ini file in the \modeltech directory (or the modelsim.ini file in your current directory if one exists) to specify a command that is to be executed after the design is loaded. To do this, open

```
<install_dir>\modeltech\modelsim.ini
```

using a text editor and uncomment the following line (by deleting the leading ;) in the [vsim] section of the file:

```
Startup = do startup.do
```

Then save *modelsim.ini*.

- ▶ **Note:** The *modelsim.ini* file must be write-enabled for this change to take place. Using MS Explorer, right-click on \<install_dir>\modeltech\modelsim.ini, then click Properties. In the dialog box, uncheck the Read-only box and click OK. (You can also copy the file to your current directory.)

- 3 Take a look at the DO file. It uses the predefined variable **\$entity** to do different things at startup for different designs.

- 4 Start the simulator and specify the top-level design unit to be simulated by entering the following command at the UNIX/DOS prompt:

```
vsim counter
```

Notice that the simulator loads the design unit without displaying the Load Design dialog box. This is handy if you are simulating the same design unit over and over. Also notice that all the windows are open. This is because the **view *** command is included in the startup macro.

- 5 If you plan to continue with the following practice sessions, keep ModelSim running. If you would like to quit the simulator, enter the following command at the VSIM prompt:

```
quit -f
```

- 6 You won't need the *startup.do* file for any other examples, so use your text editor to comment out the "Startup" line in *modelsim.ini*.

Lesson 8 - Finding names and values

The goals for this lesson are:

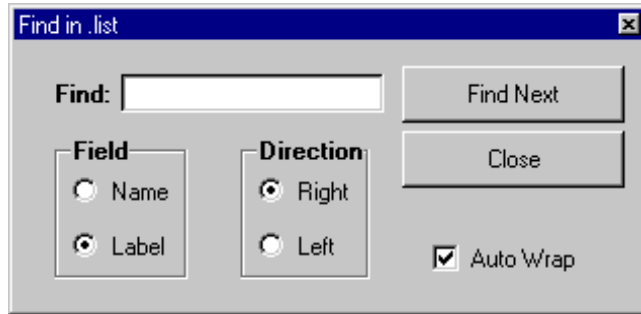
- Find items by name in tree windows
- Search for item values in the List and Wave windows

Start any of the lesson simulations to try out the Find and Search functions illustrated below.

Finding items by name in tree windows

You can find HDL item names with the **Edit > Find** menu selection in these windows: List, Process, Signals, Source, Structure, Variables, and Wave windows.

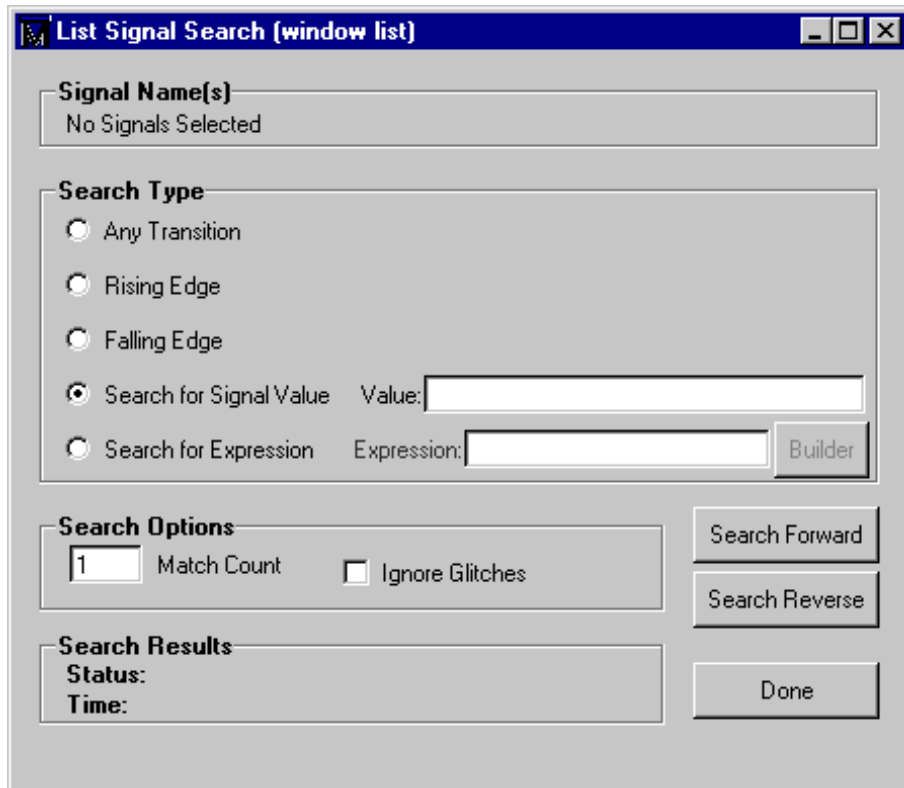
Select **Edit > Find** to bring up the Find dialog box (List window version shown).



Enter an item label and **Find** it by searching **Right** or **Left** through the window display.

Searching for item values in the List and Wave windows

You can search for HDL item values in the List and Wave windows. Select **Edit > Search** from the window's menu to bring up the Signal Search dialog box (List window version shown).



You can locate values for the **Signal Name(s)** shown at the top of the dialog box. The search is based on these options:

- **Search Type: Any Transition**
Searches for any transition in the selected signal(s).
- **Search Type: Rising Edge**
Searches for rising edges in the selected signal(s).
- **Search Type: Falling Edge**
Searches for falling edges in the selected signal(s).
- **Search Type: Search for Signal Value**
Searches for the value specified in the **Value** field; the value should be formatted using VHDL or Verilog numbering conventions.

- **Search Type: Search for Expression**
Searches for the expression specified in the **Expression** field evaluating to a boolean true. Activates the **Builder** button so you can use the Expression Builder if desired.

The expression may involve more than one signal but is limited to signals logged in the List window. Expressions may include constants, variables, and Tcl macros. If no expression is specified, the search will give an error. See the *ModelSim Command Reference* for more information on expression syntax.

- **Search Options: Match Count**
You can search for the n-th transition or the n-th match on value; **Match Count** indicates the number of transitions or matches to search.
- **Search Options: Ignore Glitches**
Ignore zero width glitches in VHDL signals and Verilog nets.

The result of your search is indicated at the bottom of the dialog box.

Lesson 9 - Using the Wave window

The goals for this lesson are:

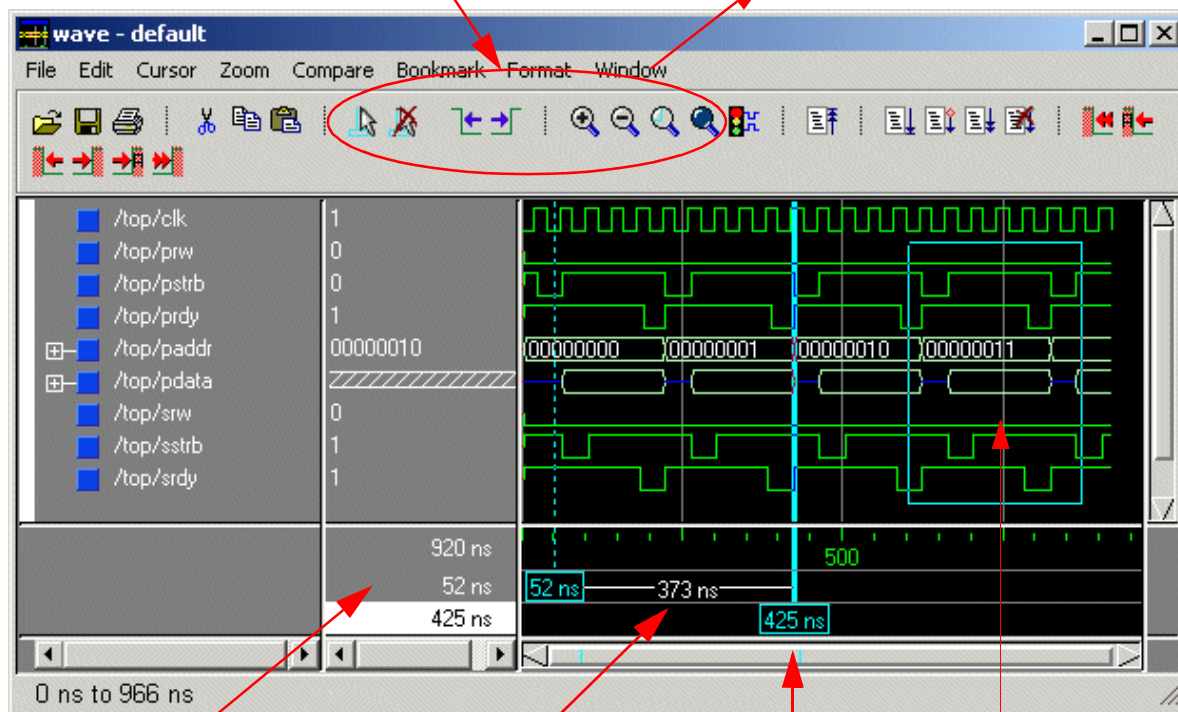
- Practice using the Wave window time cursors.
- Practice zooming the waveform display.
- Practice using Wave window keyboard shortcuts.
- Practice combining items into a virtual object.
- Practice creating and viewing datasets.

Any of the previous lesson simulations may be used with this practice, or use your own simulation if you wish.

Using time cursors in the Wave window

When the Wave window is first drawn, there is one cursor located at time zero. Clicking anywhere in the waveform display brings that cursor to the mouse location.

These Wave window buttons give you quick access to cursor placement and zooming.



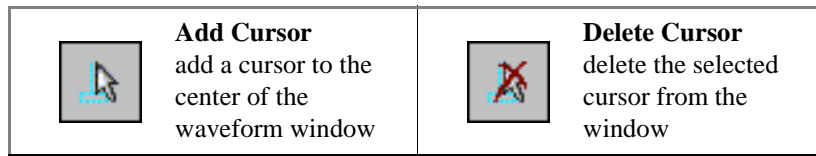
click a value here to scroll the window to that value

interval measurement

selected cursor is bold

Click and drag with the center mouse button to zoom in on an area of the display.

You can add up to 20 cursors to the waveform pane by selecting **Cursor > Add Cursor** (or the Add Cursor button shown below). The selected cursor is drawn as a bold solid line; all other cursors are drawn with thin dashed lines. Remove cursors by selecting them and choosing using the **Cursor > Delete Cursor** menu selection (or the Delete Cursor button shown below).



Finding a cursor

The cursor value (on the **Goto** list) corresponds to the simulation time of that cursor. Choose a specific cursor view with **Cursor > Goto** menu selection.

Making cursor measurements

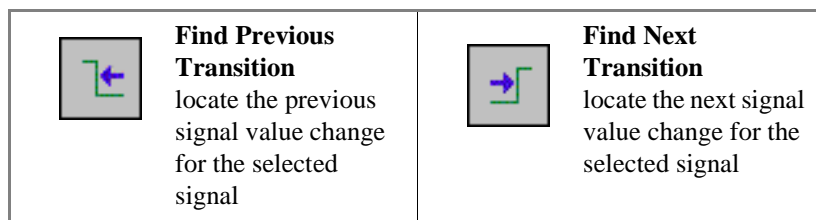
Each cursor is displayed with a time box showing the precise simulation time at the bottom. When you have more than one cursor, each time box appears in a separate track at the bottom of the display. ModelSim also adds a delta measurement showing the time difference between two adjacent cursor positions.

If you click in the waveform display, the cursor closest to the mouse position is selected and then moved to the mouse position. Another way to position multiple cursors is to use the mouse in the time box tracks at the bottom of the display. Clicking anywhere in a track selects that cursor and brings it to the mouse position.

The cursors are designed to snap to the closest wave edge to the left on the waveform that the mouse pointer is positioned over. To modify the snap distance, select **Edit > Display Properties** (Wave window).

You can position a cursor without snapping by dragging in the area below the waveforms.

You can also move cursors to the next transition of a signal with these toolbar buttons:



Zooming - changing the waveform display range

Zooming lets you change the simulation range in the waveform display. You can zoom with either the **Zoom** menu, toolbar buttons, mouse, keyboard, or commands.

Using the Zoom menu

You can use the Wave window menu bar, or call up the **Zoom** menu by clicking the right mouse button (of a three-button mouse) in the waveform pane.





- ▶ **Note:** The right mouse button of a two-button mouse will not open the **Zoom** menu. It will, however, allow you to create a zoom area by dragging left to right while holding down the button.

The Zoom menu options include:

- **Zoom Full**
Redraws the display to show the entire simulation from time 0 to the current simulation time.
- **Zoom In**
Zooms in by a factor of two, increasing the resolution and decreasing the visible range horizontally.
- **Zoom Out**
Zooms out by a factor of two, decreasing the resolution and increasing the visible range horizontally.
- **Zoom Last**
Restores the display to where it was before the last zoom operation.
- **Zoom Area with Mouse Button 1**
Use mouse button 1 to create a zoom area. Position the mouse cursor to the left side of the desired zoom interval, press mouse button 1 and drag to the right. Release when the box has expanded to the right side of the desired zoom interval.
- **Zoom Range**
Brings up a dialog box that allows you to enter the beginning and ending times for a range of time units to be displayed.

Zooming with the toolbar buttons

These zoom buttons are available on the toolbar:

 <p>Zoom in 2x zoom in by a factor of two from the current view</p>	 <p>Zoom area use the cursor to outline a zoom area</p>
 <p>Zoom out 2x zoom out by a factor of two from current view</p>	 <p>Zoom Full zoom out to view the full range of the simulation from time 0 to the current time</p>

Zooming with the mouse

To zoom with the mouse, position the mouse cursor to the left side of the desired zoom interval, press the middle mouse button (three-button mouse), or right button (two-button mouse), and while continuing to press, drag to the right and then release at the right side of the desired zoom interval.

Keyboard shortcuts for zooming

Using the following keys when the mouse cursor is within the Wave window will cause the indicated actions:

Key	Action
i I or +	zoom in
o O or -	zoom out
f or F	zoom full
l or L	zoom last
r or R	zoom range
<arrow up>	scroll waveform display up
<arrow down>	scroll waveform display down
<arrow left>	scroll waveform display left
<arrow right>	scroll waveform display right
<page up>	scroll waveform display up by page
<page down>	scroll waveform display down by page
<tab>	searches forward (right) to the next transition on the selected signal

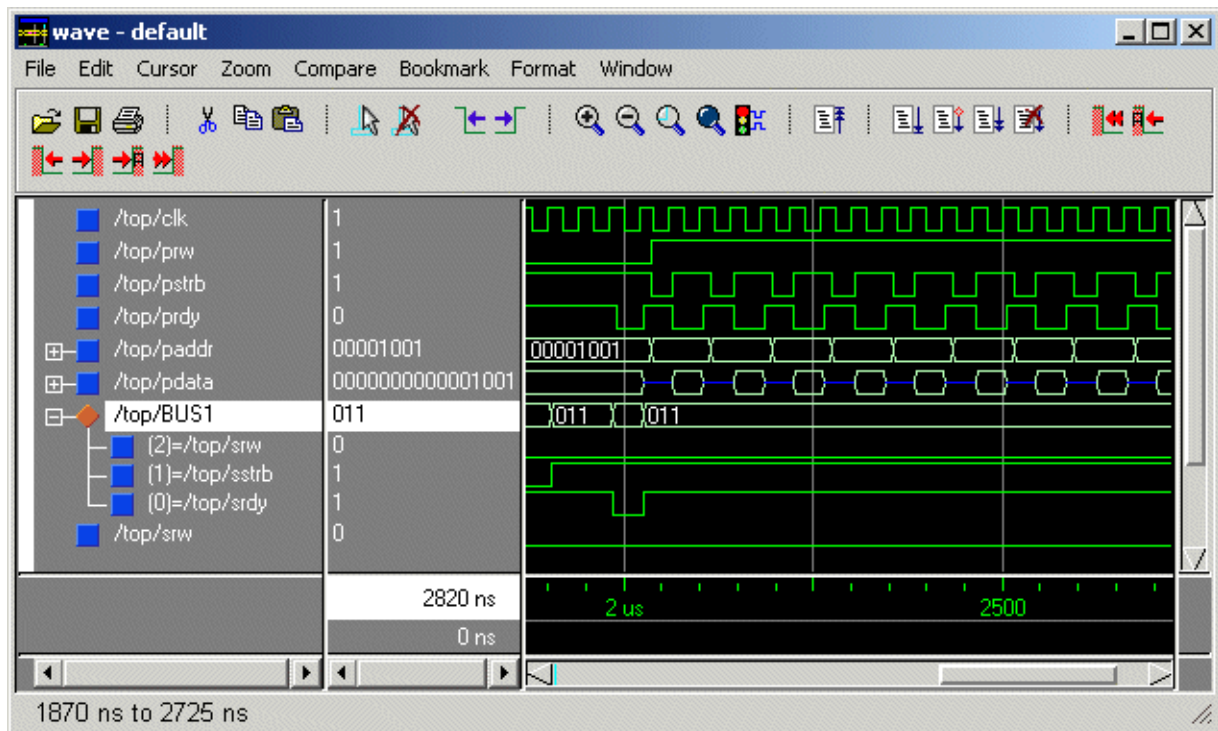
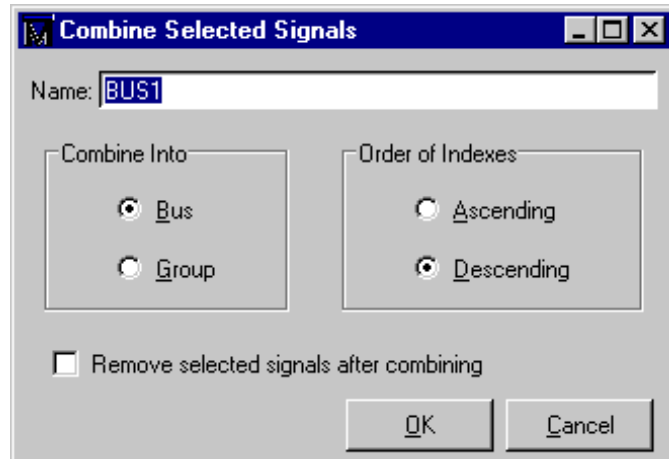
Key	Action
<shift-tab>	searches backward (left) to the previous transition on the selected signal
<Control-f> (Windows) <Control-s> (UNIX)	opens the find dialog box; searches within the specified field in the pathname pane for text strings

Combining items in the Wave window

The Wave window allows you to combine signals into buses or groups. Use the **Edit > Combine** menu selections to call up the Combine Selected Signals Dialog box.

A bus is a collection of signals concatenated in a specific order to create a new virtual signal with a specific value.

In the illustration below, three data signals have been combined to form a new bus called BUS1. Notice, the new bus has a value that is made up of the values of its component signals arranged in a specific order. Virtual objects are indicated by an orange diamond.



Creating and viewing datasets

Datasets allow you to view previous simulations or to compare simulations. To view a dataset, you must first save a ModelSim simulation to a WLF file (using the **vsim -wlf** command). Once you have saved a WLF file, you can open it as a view-mode dataset.

In this lesson you will compare two simple Verilog designs: a structural description and an RTL description of a 4-bit, binary counter. To begin, you will simulate the structural description and save it to a WLF file. Then you will simulate the RTL version. Finally, you will open the WLF file as a dataset and compare the two simulations in the Wave window.

Simulating the structural version

- 1 Start by creating a new working directory, making it the current directory, and copying the files from `\modeltech\examples\datasets` into it.

- 2 Use the **vlib** command to create a **work** library in the current directory.

```
vlib work
```

(MENU: Design > Create a New Library)

- 3 Use the **vmap** command to map the work library to a physical directory. A *modelsim.ini* file will be written into the **work** directory.

```
vmap work work
```

- 4 Compile the structural version of the counter.

```
vlog cntr_struct.v
```



(MENU: Design > Compile)

- 5 Load the design and save the simulation to a WLF file named *struct.wlf*.

```
vsim -wlf struct.wlf work.cntr_struct
```

- 6 Now you will run a DO file that applies stimulus to the design, runs the simulation, and adds waves to the Wave window.

```
do stimulus.do
```

(MENU: Macro > Execute Macro)

The waves that appear in the Wave window are saved automatically into the *struct.wlf* file.

- 7 Quit the simulation.

```
quit -sim
```

(MENU: Design > End Simulation)

Simulating the RTL version

- 1 Compile the RTL version of the counter.

```
vlog cntr_rtl.v
```

- 2 Simulate the design.

```
vsim work.cntr_rtl
```



(MENU: Design > Load Design)

- 3 Run a DO file to apply stimulus to the design.

```
do stimulus.do
```

Comparing the two designs

To compare the two simulations, we will create a second pane in the Wave window, open the *struct.wlf* file, and add the signals from the dataset to the new pane.

- 1 Add a second pane to the Wave window.

MENU: Wave > File > New Window Pane

Notice that a thick, white vertical bar at the left edge of the window indicates that the new pane is active. You probably want to increase the height of this new pane by pointing at the top border of the pane and clicking and dragging with the two-headed arrow.

- 2 Open *struct.wlf* (if you don't specify a dataset name, it will be named "struct" by default).

```
dataset open struct.wlf
```

(MENU: Wave > File > Open Dataset)

- 3 Add signals for the "struct" dataset.

```
add wave *
```

Notice that the pathname prefix for the signals you just added is the dataset name "struct". The pathname prefix for the active simulation is "sim".

The results for each simulation should be the same. You can continue experimenting with the two simulations or quit the simulator.

```
quit -f
```

(MENU: Main > File > Quit)

Lesson 10 - Simulating with the Performance Analyzer

The goals for this lesson are:

- Compare run times with Performance Analyzer turned on and off
- View the Hierarchical and Ranked Profile displays
- Use the Performance Analyzer statistics displayed in the Hierarchical Profile and the Ranked Profile to speed up simulation

Performance Analyzer identifies the percentage of simulation time spent in each section of your code. With this information, you can identify bottlenecks and reduce simulation time by optimizing your code. Users have reported up to 75% reductions in simulation time after using Performance Analyzer.

This lesson introduces the Performance Analyzer and shows you how to use the main Performance Analyzer commands.

- ▶ **Note:** You must be using ModelSim SE to complete this lesson. Also, Performance Analyzer *will not* operate on Windows 95.

Preparing the simulation

This lesson will use an example design that contains lower level VHDL blocks in the files *control.vhd*, *retrieve.vhd*, and *store.vhd*; and top level block, test bench and configuration files – *ringrtl.vhd*, *testring.vhd*, and *config_rtl.vhd*.

- 1 Start by creating a new working directory, making it the current directory, and copying the files from `\modeltech\examples\profiler` into it.

- 2 Use the **vlib** command to create a **work** library in the current directory.

```
vlib work
```

(MENU: Design > Create a New Library)

- 3 Use the **vmap** command to map the work library to a physical directory. A *modelsim.ini* file will be written into the **work** directory.

```
vmap work work
```

- 4 Compile the lower level blocks of the design.

```
vcom control.vhd retrieve.vhd store.vhd
```



(MENU: Design > Compile)

- 5 Compile the top level block, test bench and configuration files.

```
vcom ringrtl.vhd testring.vhd config_rtl.vhd
```



(MENU: Design > Compile)

- 6 Use the **vsim** command to load the design configuration.

```
vsim work.test_bench_rtl
```

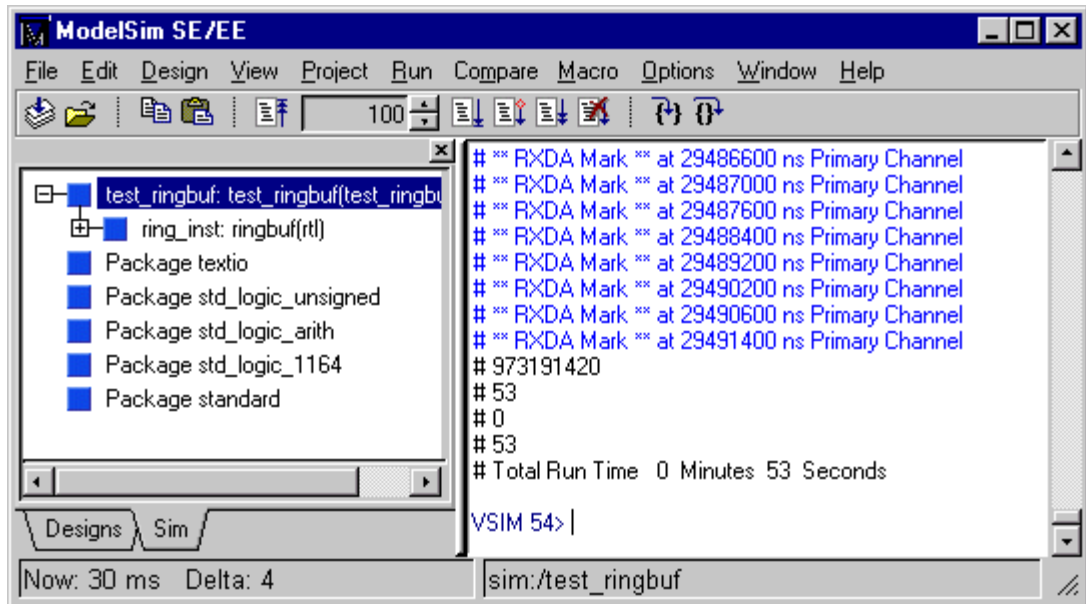


(MENU: Design > Load Design)

Running the simulation

- 1 Now, run the supplied DO file – *timerun.do*. This file runs the simulation and displays the total run time in the transcript area of the Main window. This test should take a minute or two.

```
do timerun.do
```



Take a look at the commands in the *timerun.do* file. The *seconds* Tcl command is used to time the simulation.

Make a note of the run time of the simulation. (Your run time will depend on the processing speed of your system and may differ from the run time shown here.)

Now we'll reset the simulation to time zero so that the simulation can be timed with the Performance Analyzer ON. This will show you how little overhead there is in running a simulation with the Performance Analyzer enabled.

- 2 Restart the simulation

```
restart -f
```



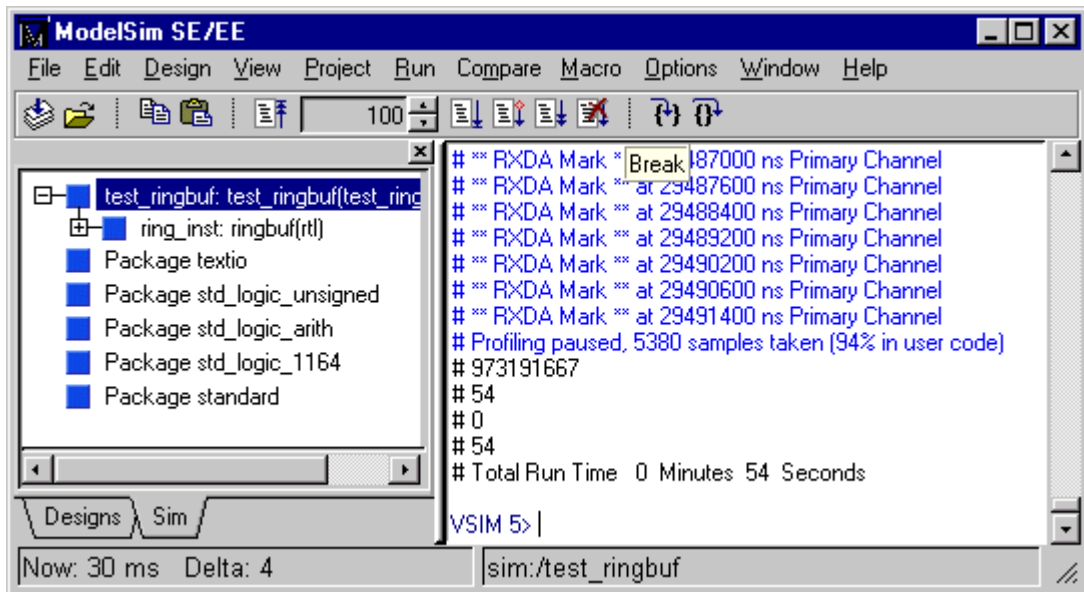
- 3 Use the **profile on** command to turn on the Performance Analyzer.

```
profile on
```

- 4 Now use the *timerun.do* file again to run the simulation.

```
do timerun.do
```

Notice that the overhead of running the Performance Analyzer is very small (your results may differ from the results shown here), even with over 5000 samples of the simulation run acquired.



5 Display the Hierarchical Profile output.

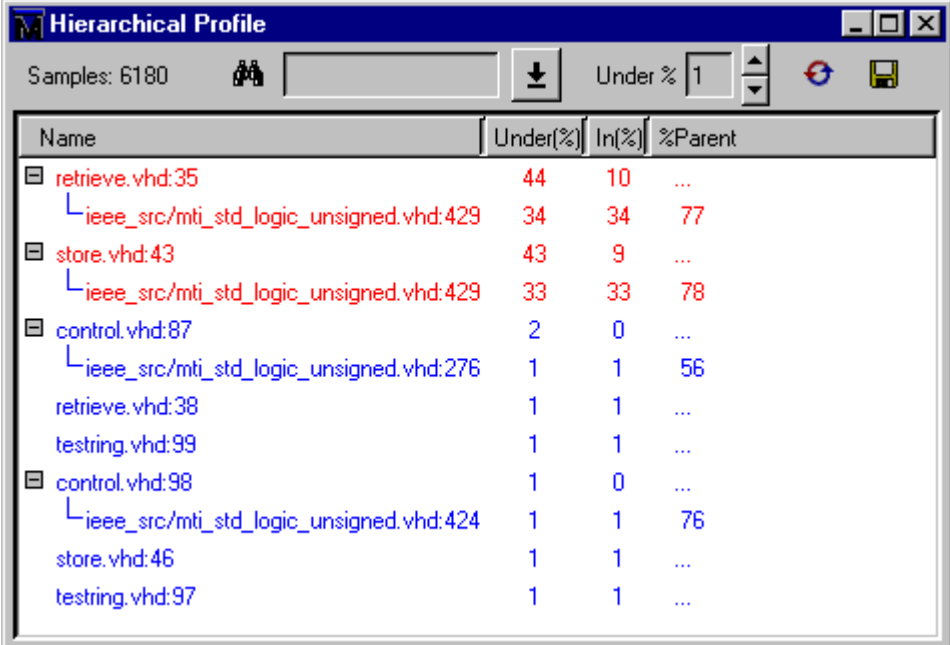
```
view_profile
```

(MENU: View > Other > Hierarchical Profile)

Note that two lines – *retrieve.vhd:35* and *store.vhd:43* – are taking the majority of the simulation time.

You can use the $\$PrefProfile(hierCutoff)$ Tcl control variable to filter out everything below a certain percentage. **hierCutoff** is the minimum percent usage that will be listed in the Hierarchical Profile display. The default value is 1%. Any usage less than 1% will not be displayed.

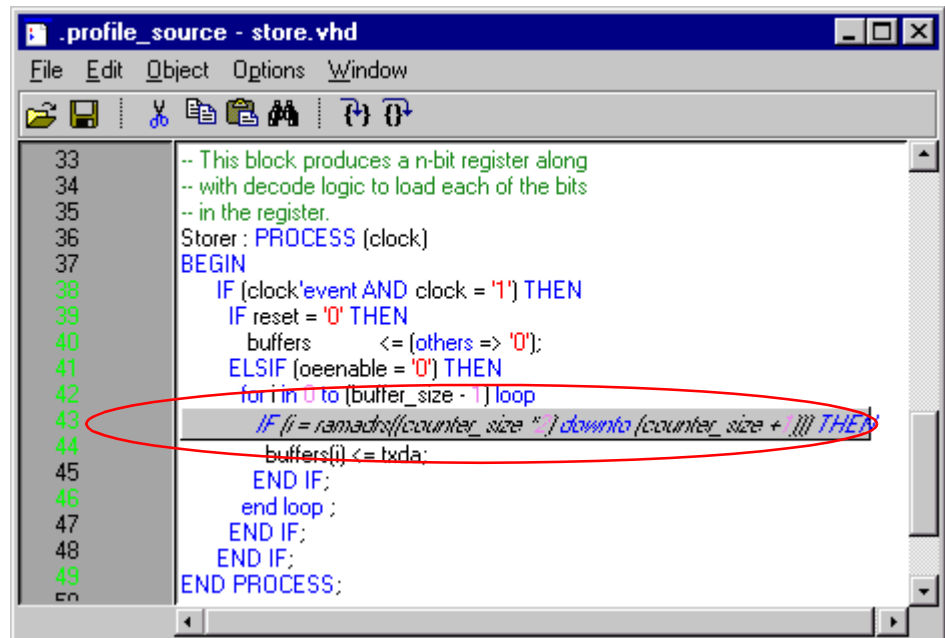
You can also filter the display with the Under % filter in the Hierarchical Profile window.



The screenshot shows the 'Hierarchical Profile' window with a table of simulation components. The table has four columns: Name, Under(%), In(%), and %Parent. The data is as follows:

Name	Under(%)	In(%)	%Parent
retrieve.vhd:35	44	10	...
└ ieee_src/mti_std_logic_unsigned.vhd:429	34	34	77
store.vhd:43	43	9	...
└ ieee_src/mti_std_logic_unsigned.vhd:429	33	33	78
control.vhd:87	2	0	...
└ ieee_src/mti_std_logic_unsigned.vhd:276	1	1	56
retrieve.vhd:38	1	1	...
testring.vhd:99	1	1	...
control.vhd:98	1	0	...
└ ieee_src/mti_std_logic_unsigned.vhd:424	1	1	76
store.vhd:46	1	1	...
testring.vhd:97	1	1	...

Double-clicking on any line in the Hierarchical Profile window will open the Source window and allow you to view the relevant source code for that line. The selected line will be highlighted in the Source window as shown below. (Here, we've double-clicked *store.vhd:43*.)



```
.profile_source - store.vhd
File Edit Object Options Window
-- This block produces a n-bit register along
-- with decode logic to load each of the bits
-- in the register.
Storer : PROCESS (clock)
BEGIN
  IF (clock'event AND clock = '1') THEN
    IF reset = '0' THEN
      buffers <= (others => '0');
    ELSIF (oenable = '0') THEN
      for i in 0 to (buffer_size - 1) loop
        IF (i = ramaddr((counter_size * ) downto (counter_size + ))) THEN
          buffers(i) <= txda;
        END IF;
      end loop ;
    END IF;
  END IF;
END PROCESS;
```

Speeding up the simulation

The information provided by the Performance Analyzer can be used to speed up the simulation. Double click the pathname for *store.vhd:43* and *retrieve.vhd:35* and view the source code. In both cases, the source includes a loop which could have an exit.

- 1 Modify the loops to include exits inside the *IF* statements, or compile the following files included for that purpose – *store_exit.vhd* and *retrieve_exit.vhd*.

```
vcom retrieve_exit.vhd store_exit.vhd
```



(MENU: Design > Compile)

- 2 Compile the top level blocks and configuration files again to account for the lower level changes.

```
vcom ringrtl.vhd teststring.vhd config_rtl.vhd
```



(MENU: Design > Compile)

- 3 Reset the simulation to time zero and restart with the modified files.

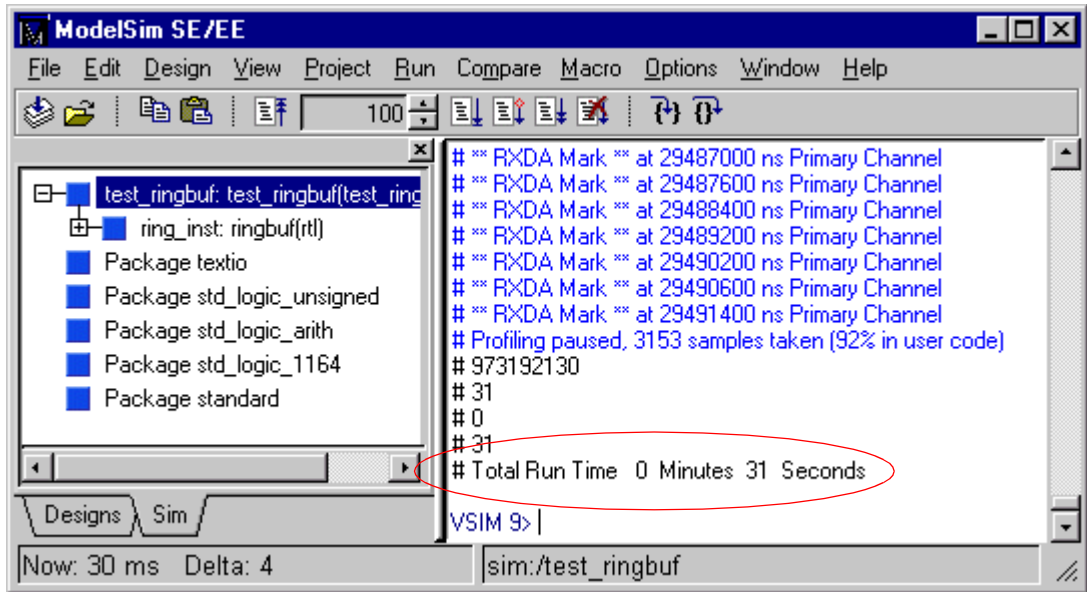
```
restart -f
```



- 4 Run `timerun.do` again and note the difference in run time.

```
do timerun.do
```

Run time has been cut almost in half by inserting exits in the loops.

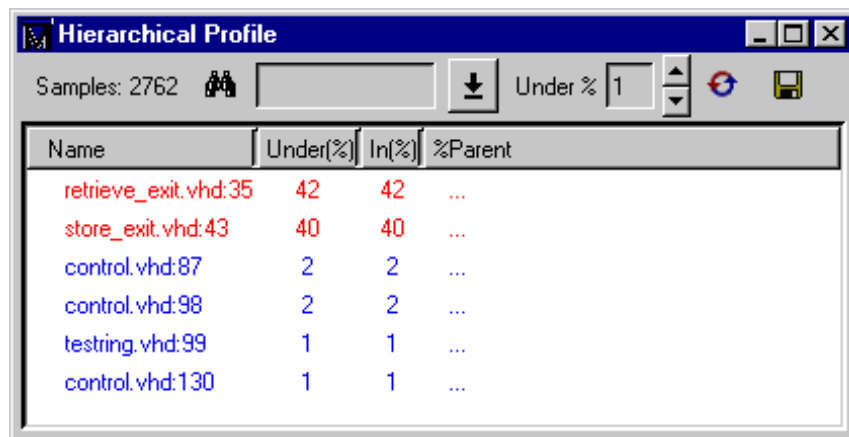


- 5 Take another look at the Performance Analyzer data.

```
view_profile
```

(MENU: View > Other > Hierarchical Profile)

A lot of time is still being spent in the loops. To further reduce simulation time, these loops can be replaced by indexing an array.



- 6 Remove the loops and add an array, or compile the following files with the modifications already done.

```
vcom retrieve_array.vhd store_array.vhd
```



(MENU: Design > Compile)

- 7 Compile the top level blocks and configuration files again.

```
vcom ringrtl.vhd testring.vhd config_rtl.vhd
```



(MENU: Design > Compile)

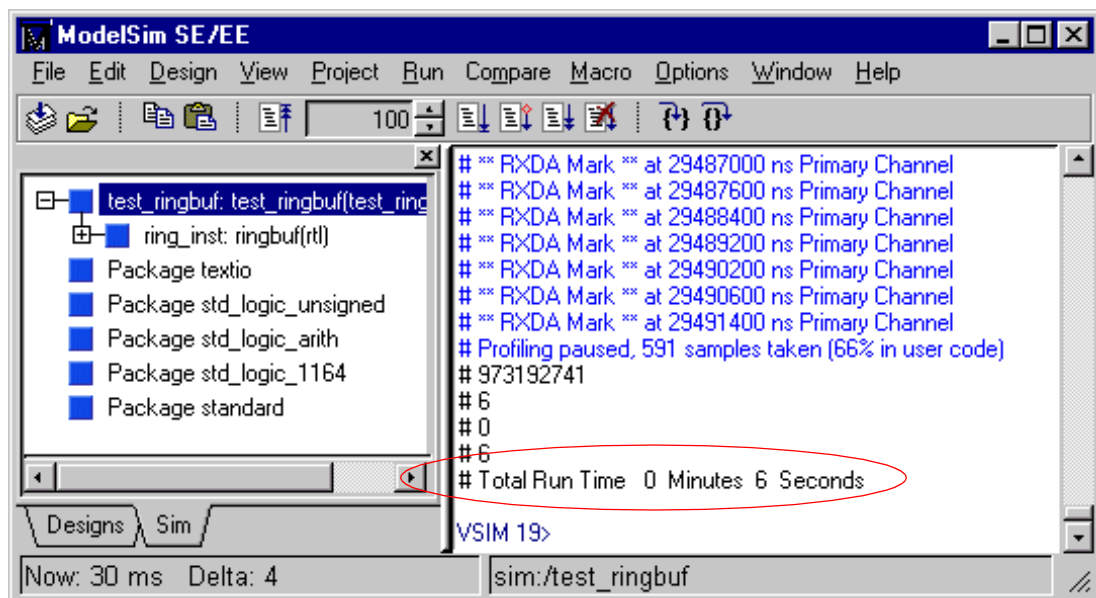
- 8 Restart the simulation with the modified files.

```
restart -f
```



- 9 Run *timerun.do* again and note the difference in simulation run time. Your simulation time may differ from that shown here, but the new run should be very fast – approximately ten times faster than the original simulation time.

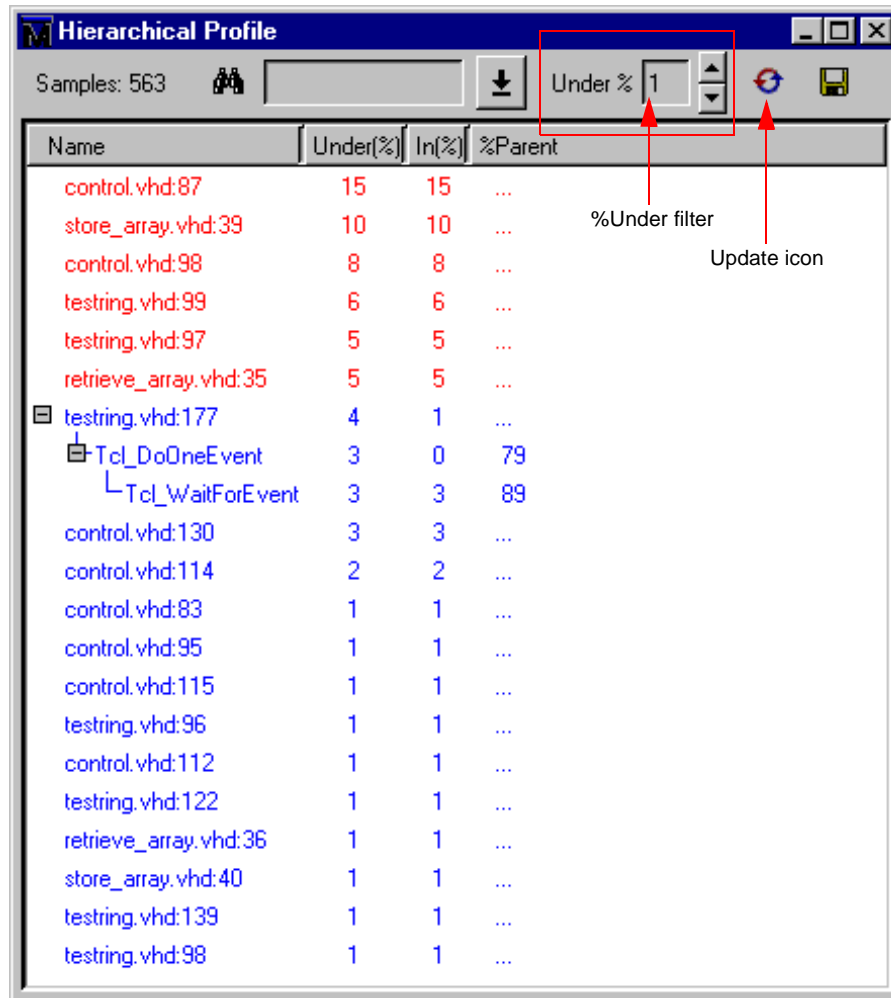
```
do timerun.do
```



- 10 Look, again, at the Hierarchical Profile of simulation performance and you will see more lines showing.

view_profile

(MENU: View > Other > Hierarchical Profile)



- **Note:** Your results may look slightly different as a result of the computer you're using and different system calls that occur during the simulation.

- 11 Set the Under% filter to "2" and click the Update icon. This will filter out all usage values below 2%.

The screenshot shows the 'Hierarchical Profile' window. The 'Under %' filter is set to 2. The table below shows the filtered data:

Name	Under(%)	In(%)	%Parent
control.vhd:87	15	15	...
store_array.vhd:39	10	10	...
control.vhd:98	8	8	...
testring.vhd:99	6	6	...
testring.vhd:97	5	5	...
retrieve_array.vhd:35	5	5	...
testring.vhd:177	4	1	...
Tcl_DoOneEvent	3	0	79
Tcl_WaitForEvent	3	3	89
control.vhd:130	3	3	...
control.vhd:114	2	2	...

- 12 Take a look at the Ranked Profile view.

view_profile_ranked

(MENU: View > Other > Ranked Profile)

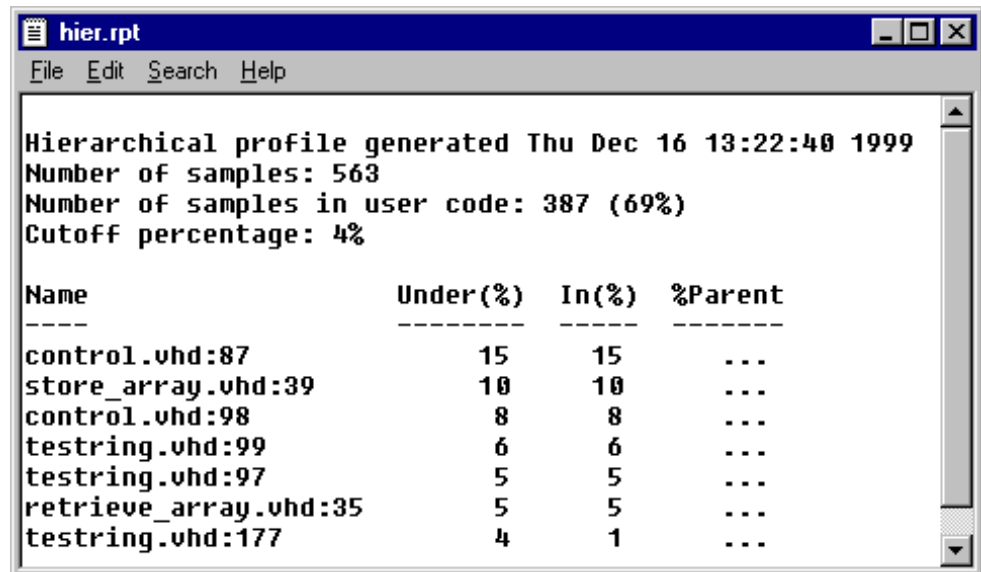
The screenshot shows the 'Ranked Profile' window. The 'In %' filter is set to 4. The table below shows the ranked data:

Name	Under(%)	In(%)
control.vhd:87	15	15
store_array.vhd:39	10	10
control.vhd:98	8	8
testring.vhd:99	6	6
testring.vhd:97	5	5
retrieve_array.vhd:35	5	5
Tcl_WaitForEvent	3	3
control.vhd:130	3	3
control.vhd:114	2	2

- 13 Use the report command to output a file with the profile data.

```
profile report -hierarchical -file hier.rpt -cutoff 4
```

This command outputs a hierarchical profile of performance data with the file name *hier.rpt*.



The screenshot shows a text window titled "hier.rpt" with a menu bar containing "File", "Edit", "Search", and "Help". The main content of the window is a hierarchical profile report generated on Thursday, December 16, 1999, at 13:22:40. The report includes the following summary statistics:

- Hierarchical profile generated Thu Dec 16 13:22:40 1999
- Number of samples: 563
- Number of samples in user code: 387 (69%)
- Cutoff percentage: 4%

Below the summary statistics is a table with the following columns: Name, Under(%), In(%), and %Parent. The table contains the following data:

Name	Under(%)	In(%)	%Parent
control.vhd:87	15	15	...
store_array.vhd:39	10	10	...
control.vhd:98	8	8	...
teststring.vhd:99	6	6	...
teststring.vhd:97	5	5	...
retrieve_array.vhd:35	5	5	...
teststring.vhd:177	4	1	...

- 14 Quit the simulator.

```
quit -f
```

Lesson 11 - Simulating with Code Coverage

The goals for this lesson are:

- Run a simulation with Code Coverage ON and examine the coverage_summary window
- Save line coverage information to a text file
- Exclude lines and files from the coverage statistics
- Append results from a previous simulation run onto the next one

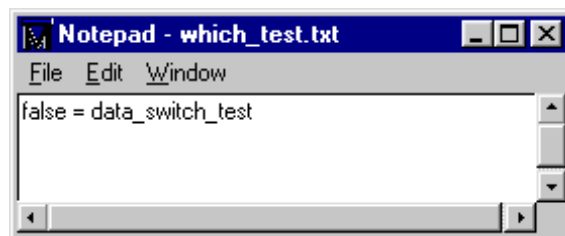
ModelSim Code Coverage allows you to identify which lines in your code are being covered by the testbench. It is non-intrusive (instrumented code is *not* required) and only minimally impacts simulation performance (<5%).

Running a simulation with Code Coverage

All commands are shown as entered on the ModelSim command line.

For this lesson, you'll use the same working directory used for the Simulating with the Performance Analyzer lesson. It is not necessary to recreate the work library if you completed the last lesson. See [Lesson 10 - Simulating with the Performance Analyzer](#) (T-77) if you need the details on these steps.

- 1 Prior to running the simulation, we need to check the *which_test.txt* file in the *modeltech\examples\profiler* directory to ensure it reads "false = data_switch_test". You can edit the file with **notepad** within ModelSim.



This switch configures the test bench – the *ringrtl.vhd* file. We'll change it later in the lesson when we merge the coverage results of two simulations.

- 2 Compile the lower level blocks of the design.

```
vcom control.vhd retrieve.vhd store.vhd
```



(MENU: Design > Compile)

- 3 Compile the top level block, test bench, and configuration files.

```
vcom ringrtl.vhd teststring.vhd config_rtl.vhd
```



(MENU: Design > Compile)

- 4 Use the **vsim -coverage** command to load the design configuration with Code Coverage.

```
vsim -coverage work.test_bench_rtl
```

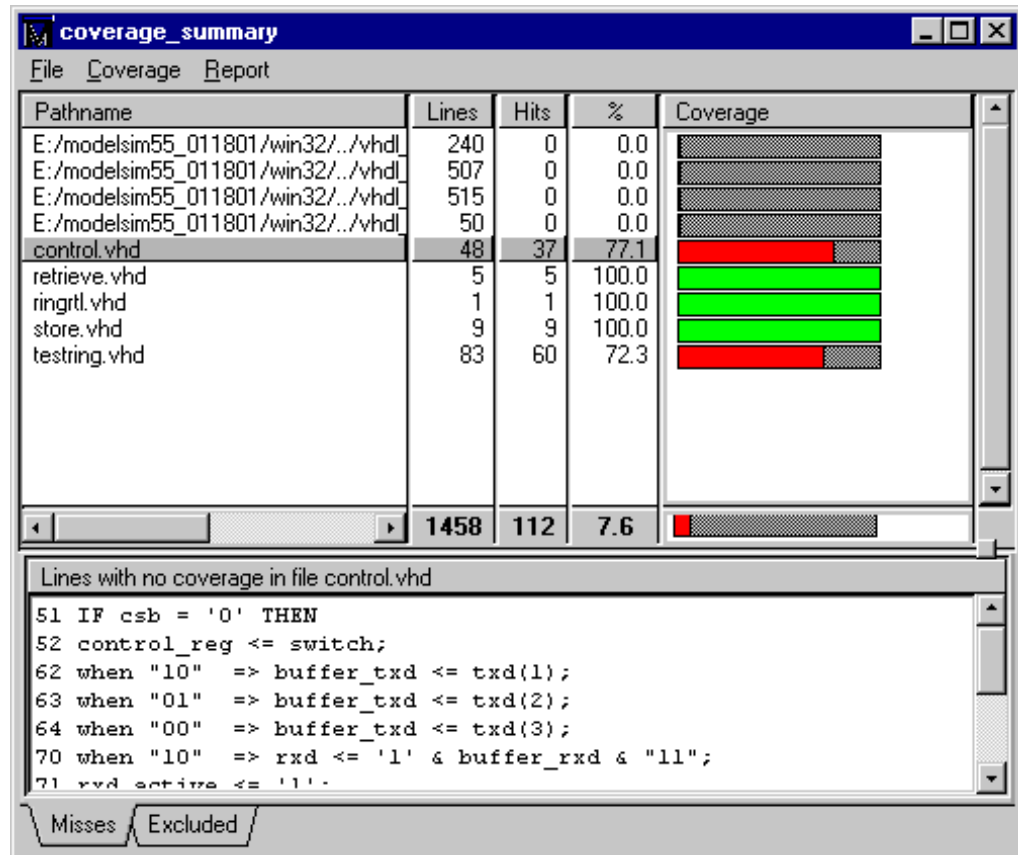
- 5 Run the simulator for 3 milliseconds.

```
run 3 ms
```

6 Display the coverage_summary window.

```
view_coverage
```

(MENU: View > Other > Source Coverage)



The top half of the window shows summary information on a per-file basis. If you select a file in the list, the bottom part of the window gives details about the lines in the file that have zero coverage.

Note that both *testing.vhd* and *control.vhd* are below 90% and, therefore, shown in red in the Coverage bar graph. 90% is the default coverage threshold, and all coverage values below 90% will be shown red. The default coverage threshold can be changed with the Tcl control variable *\$PrefCoverage(cutoff)*.

- 7 Click on the *control.vhd* pathname to display the source code for *control.vhd* in the Source window. With Code Coverage enabled, the Source window is displayed with an extra column that details the number of times each line has been executed. The green "Xs" in the graphic below denote lines that have been excluded. We'll discuss that later in the lesson.

Scroll the Source window to view the executable lines. As you can see some lines have red zeros next to them. This indicates a line that was not executed.

```

2      65      when others => buffer_txd <= 'X';
.      66
81     67      case control_reg(3 downto 2) is
79     68      when "11" => rxd <= buffer_rxd & "111";
79     69              rxd_active <= buffer_rxd;
0      70      when "10" => rxd <= '1' & buffer_rxd & "11";
X     71              rxd_active <= '1';
X     72      when "01" => rxd <= "11" & buffer_rxd & '1';
0      73              rxd_active <= '1';
0      74      when "00" => rxd <= "111" & buffer_rxd ;
0      75              rxd_active <= '1';
2      76      when others => rxd <= "XXXX"; rxd_active <= 'X';
.      77
81     78      end case;
.      79      END PROCESS;

```

- 8 Save the line coverage information to a text file.

```
coverage report -file cover.dat -lines
```

(MENU: Report > Save Line Coverage)

Open the file *cover.dat* to see how the data is stored. **Notepad** works well to check text files such as this.

```
notepad cover.dat
```


- 5 Select the line in the Excluded tab, click your right mouse button, and select **Include Entire Selected Files**. This removes the exclusion filter on any lines from the selected file.

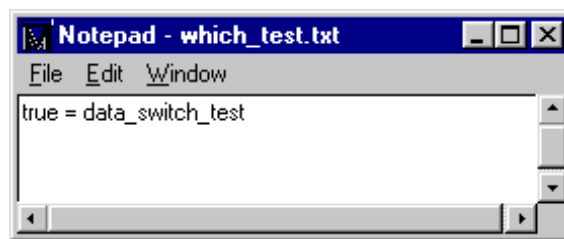
You can continue experimenting with the various exclusion commands at this point if you want. However, before continuing with the tutorial, select **Coverage > Clear Out Current Filter** to ensure all lines and files are included for the next exercise.

Merging coverage results from two simulations

You can merge code coverage results from multiple simulations. In this exercise, we'll change the test that is run by the test bench, resimulate, and then append the coverage statistics from our previous analysis to the new analysis.

- 1 Note how many times the clocked processes have been executed.
- 2 Next we'll edit the *which_test.txt* file in the *modeltech\examples\profiler* directory. Changing this text file causes a different test to be run from the same test bench. Using ModelSim Notepad, edit the file so it reads "true = data_switch_test." Make sure the **Edit > read_only** switch is not on.

```
notepad which_test.txt
```



- 3 Restart the simulation so the different test is run on the circuit.

```
restart -f
```



- 4 Restore the coverage data from the last simulation run so that its data can be appended to the current simulation.

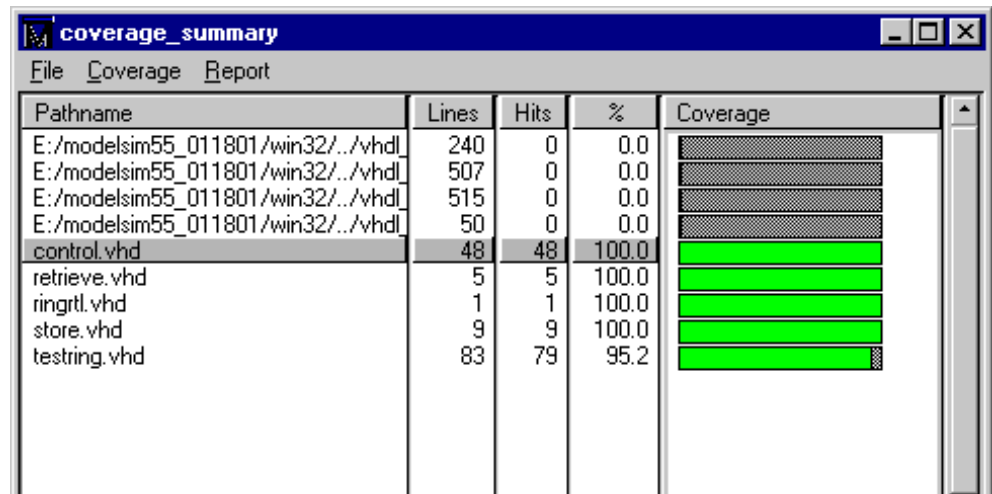
```
coverage reload cover.dat
```

(coverage_summary MENU: File > Open > Coverage > Merge Coverage)

- 5 Run the simulator for 3 milliseconds as before.

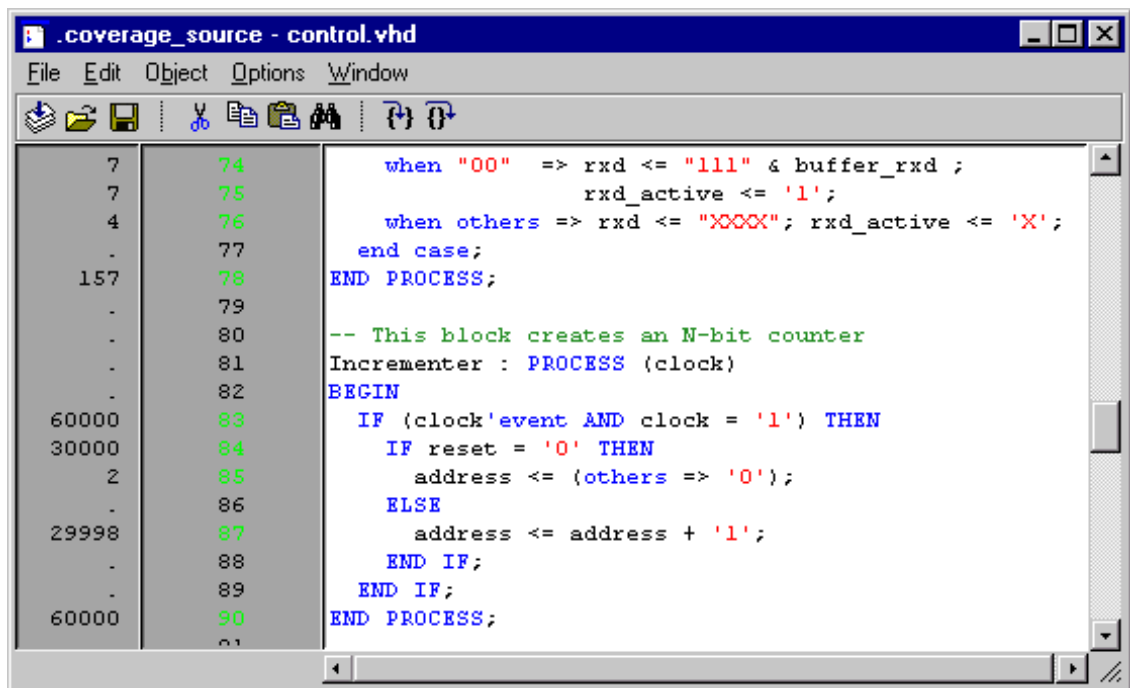
```
run 3 ms
```

Note that now both *testring.vhd* and *control.vhd* are above 90% and therefore shown in green.



Pathname	Lines	Hits	%	Coverage
E:/modelsim55_011801/win32/./vhd/	240	0	0.0	
E:/modelsim55_011801/win32/./vhd/	507	0	0.0	
E:/modelsim55_011801/win32/./vhd/	515	0	0.0	
E:/modelsim55_011801/win32/./vhd/	50	0	0.0	
control.vhd	48	48	100.0	
retrieve.vhd	5	5	100.0	
ringrtl.vhd	1	1	100.0	
store.vhd	9	9	100.0	
testring.vhd	83	79	95.2	

- Click on the *control.vhd* pathname to bring up the Source window. You can see from the values in the first column that the line hits from this run has been added to the ones from the last run. The number of times the clocked processes have been run has doubled.



```

7      74      when "00" => rxd <= "111" & buffer_rxd ;
7      75              rxd_active <= '1';
4      76      when others => rxd <= "XXXX"; rxd_active <= 'X';
.      77      end case;
.      78      END PROCESS;
157    79
.      80
.      81      -- This block creates an N-bit counter
.      82      Incrementer : PROCESS (clock)
.      83      BEGIN
60000  84      IF (clock'event AND clock = '1') THEN
30000  85      IF reset = '0' THEN
2      86          address <= (others => '0');
.      87      ELSE
29998  88          address <= address + '1';
.      89      END IF;
.      90      END IF;
60000  91      END PROCESS;

```

- Quit the simulator.
quit -f

Lesson 12 - Comparing waveforms

The goals for this lesson are:

- Compare two simulations using the Comparison Wizard
- View comparison results and timing difference markers in the Wave window
- Use compare icons to jump to "previous" and "next" difference markers
- View comparison results in the List window
- Set an edge tolerance

Waveform Comparison computes timing differences between test signals and reference signals. In this exercise we're going to run and save the mixedHDL simulation, edit one of the source files, run the simulation again, and finally compare the two runs.

The general procedure for comparing waveforms has four main steps:

- 1 Selecting the simulations or datasets to compare
- 2 Specifying the signals or regions to compare
- 3 Running the comparison
- 4 Viewing the comparison results

Creating the reference dataset

We'll start by running a simulation and saving it to a dataset. This dataset will become the reference dataset when we set up the comparison.

- 1 Start by creating a new directory for this exercise. Create the directory and copy all of the files from `\<install_dir>\modeltech\examples\mixedHDL` to the new directory.

Make sure the new directory is the current directory. Do this by invoking *ModelSim* from the new directory or by selecting the **File > Change Directory** command from the *ModelSim* Main window.

- 2 At the *ModelSim* prompt in the Transcript pane, run the `compare.do` DO file.

```
do compare.do
```

This DO file does the following:

- Creates and maps the work library
- Compiles the Verilog and VHDL files
- Runs the simulation and saves the results to a dataset named "gold.wlf"

Feel free to open the DO file and take a look at its contents.

Editing a source file and re-running the simulation

In the last step, we ran the default mixed HDL simulation and saved it to the *gold.wlf* dataset. Now we'll edit one of the source files and re-run the simulation.

- 1 Edit the *proc.v* file.

```
edit proc.v
```

- 2 Scroll down the source_edit window to line 69, and add a 10 time unit delay to the read cycle. Your source file should look like the following:



```

source_edit - proc.v
File Edit Object Options Window
[Icons]
56         verbose = 1;
57
58         forever begin
59             // Wait for first clock, then perform read/wr
60             @(posedge clk)
61             if (verbose) $display("%t: Starting Read/Writ
62
63             // Write 10 locations
64             for (a = 0; a < 10; a = a + 1)
65                 write(a, a);
66
67             // Read back 10 locations
68             for (a = 0; a < 10; a = a + 1) begin
69                 #10 read(a, d);
70                 if (d != a)
71                     $display("%t: Read/Write mismatch; E:

```

- 3 Save the file in the source_edit window.



(MENU: File > Save)

- 4 Re-compile the *proc.v* file.



(PROMPT: vlog proc.v)

(MENU: Design > Compile)

- 5 Load the top design unit.



(PROMPT: vsim work.top)

(MENU: Design > Load Design)

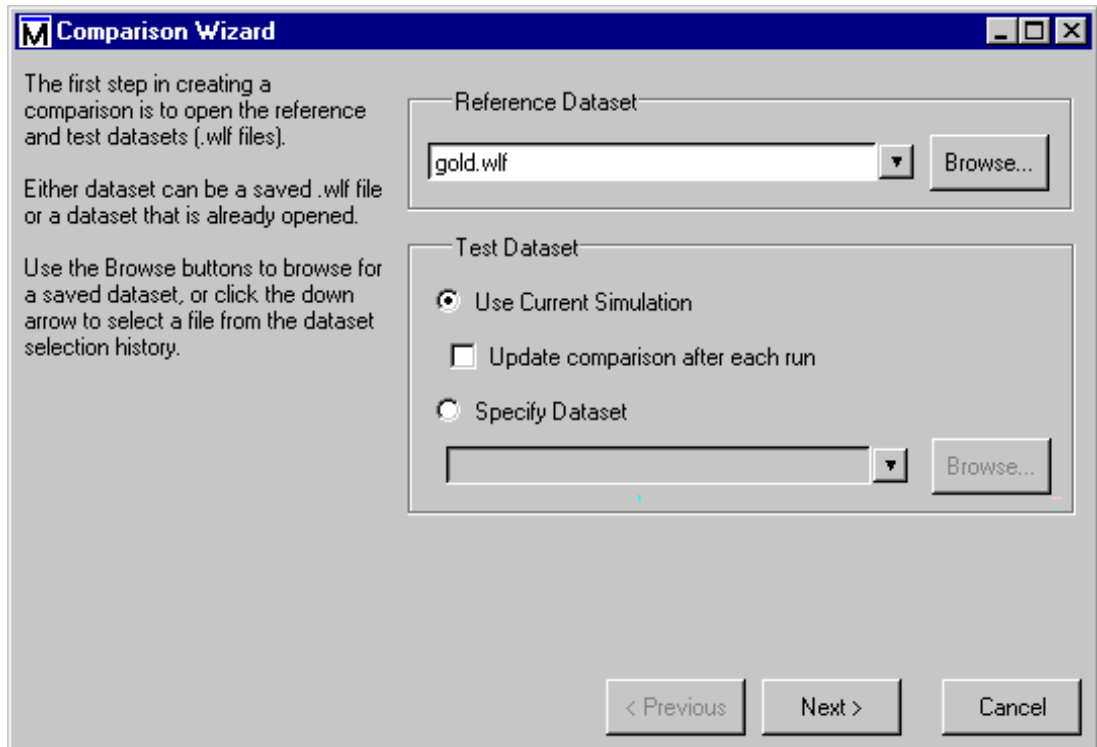
- 6 Add the waves to the Wave window and run the simulation.

```
add wave *  
run -all
```

Comparing the simulation runs

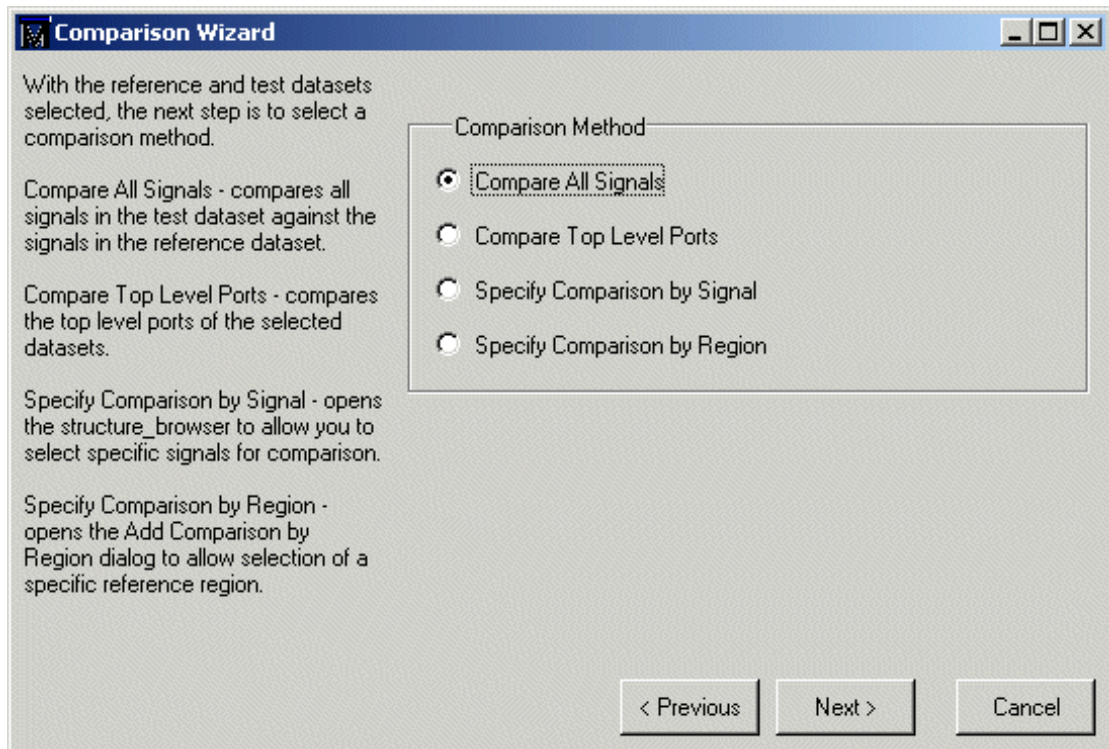
ModelSim includes a Comparison Wizard that walks you through the steps of setting up a waveform comparison. You can also do it manually with menu or command line commands.

- 1 Select **Compare > Comparison Wizard** from the Wave or Main window.
- 2 Click the browse button and select *gold.wlf* as the Reference Dataset. Recall that this dataset is from the first simulation run prior to adding the 10 time unit delay.



Leave the Test Dataset set to **Use Current Simulation**, and then click Next.

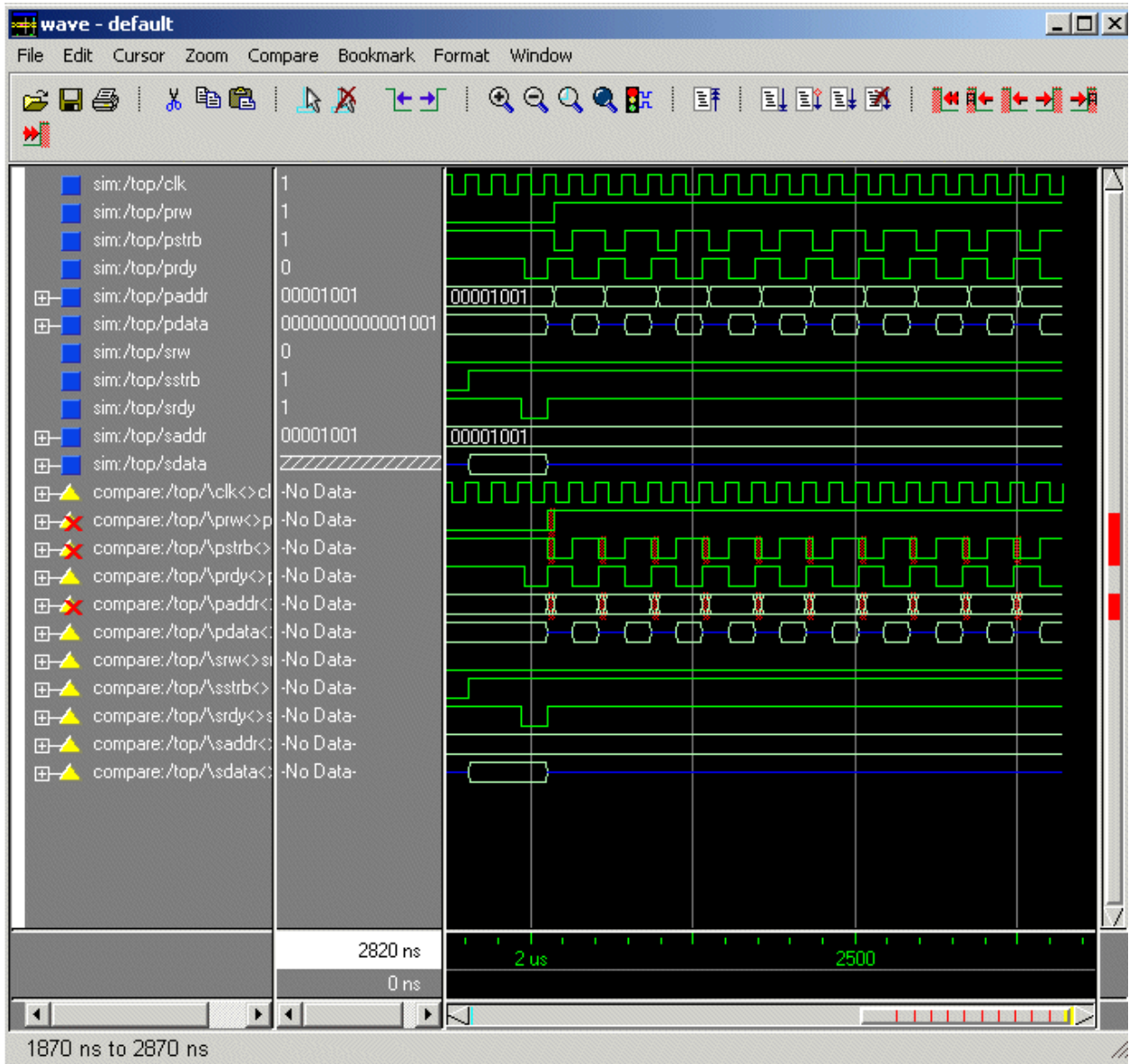
- 3 Select **Compare All Signals** in the second dialog, and then click Next.



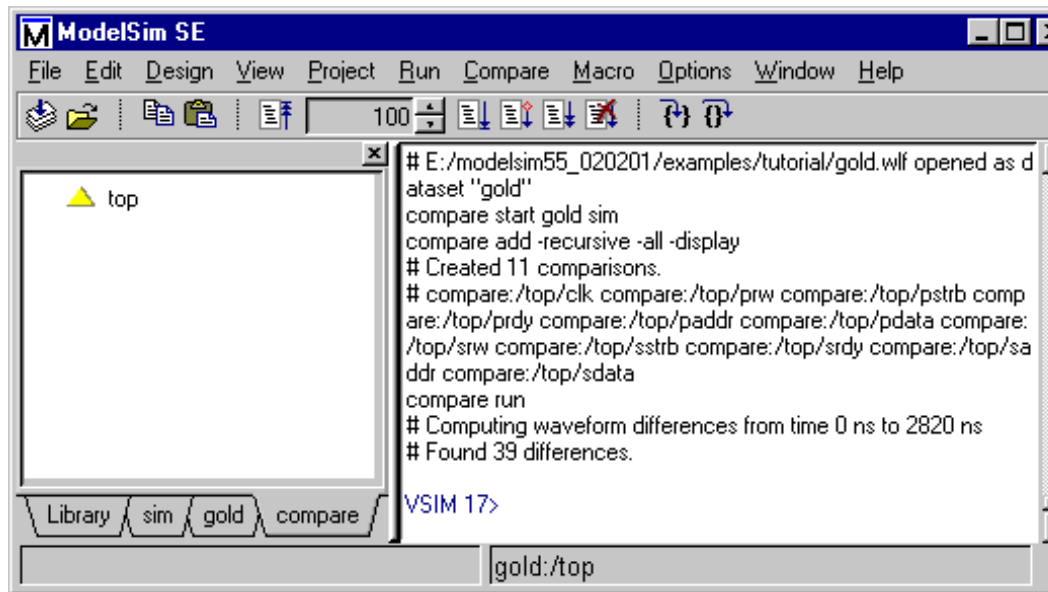
- 4 In the next three dialogs, click Next, Compute Differences Now, and Finish, respectively.

Viewing and saving the comparison data

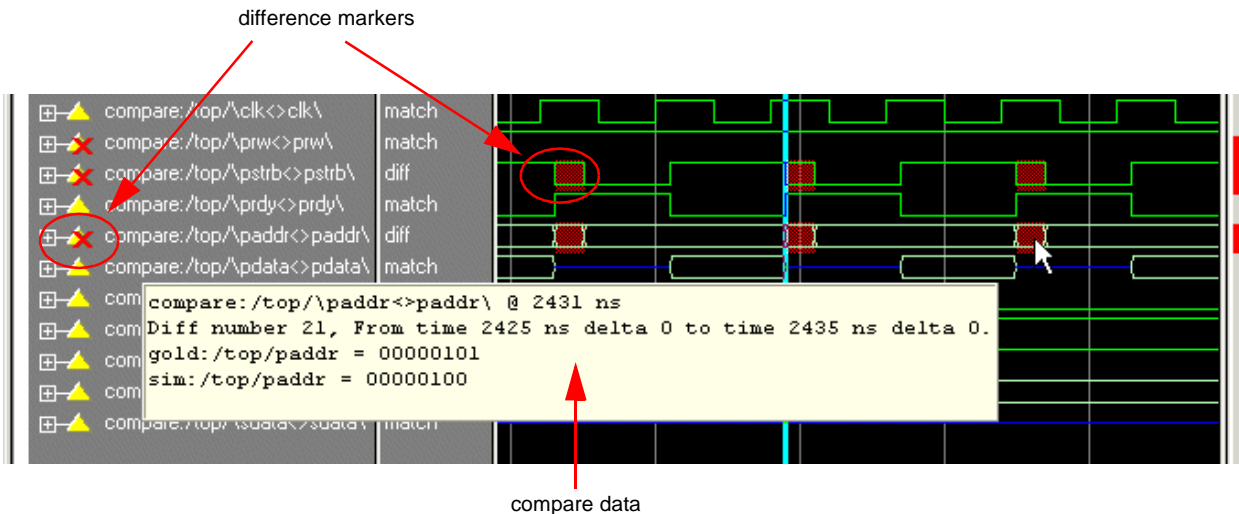
ModelSim performs the comparison and displays the compared signals in the Wave window.



The Compare tab in the Main window shows the region that was compared, and the transcript area shows the number of differences found between the timing of the Reference and Test datasets.



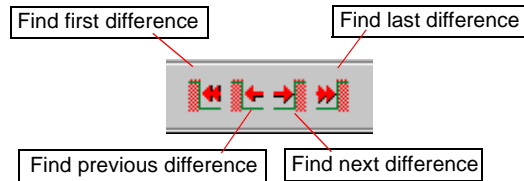
In the Wave window, a signal that contains timing differences between the two simulations is denoted by a red X over its yellow triangle. Red difference markers in the waveform display area show the location of the timing differences on the waveforms, as do the red lines in the horizontal scrollbar at the bottom of the window.



Place your cursor over a difference marker to display a popup containing data about that timing difference.

Compare icons

The Wave window includes four waveform comparison icons that let you quickly jump between differences. The next and previous buttons cycle through differences on all signals. To view differences for just the selected signal, use <tab> and <shift> - <tab>.



Use these icons to move the selected cursor. Notice that when the selected cursor is positioned over a difference marker, the values column of the signal containing the difference shows the value "diff." Otherwise, the value will show "match."

Signal	Comparison Status	Value
sim:/top/clock	match	1
sim:/top/prw	diff	0
sim:/top/pstrb	diff	1
sim:/top/prdy	match	1
sim:/top/paddr	diff	00001001
sim:/top/pdata	match	00000000000001001
sim:/top/srw	match	0
sim:/top/sstrb	match	1
sim:/top/srdy	match	1
sim:/top/saddr	match	00001001
sim:/top/sdata	match	00000000000001001
compare:/top/\clock<>cl	match	match
compare:/top/\prw<>p	diff	diff
compare:/top/\pstrb<>p	diff	diff
compare:/top/\prdy<>p	match	match
compare:/top/\paddr<>p	diff	diff
compare:/top/\pdata<>p	match	match
compare:/top/\srw<>s	match	match
compare:/top/\sstrb<>s	match	match
compare:/top/\srdy<>s	match	match
compare:/top/\saddr<>s	match	match
compare:/top/\sdata<>s	match	match

values column

Saving the comparison

You can save the comparison for later viewing, either in a text file or in files that can be reloaded into ModelSim.

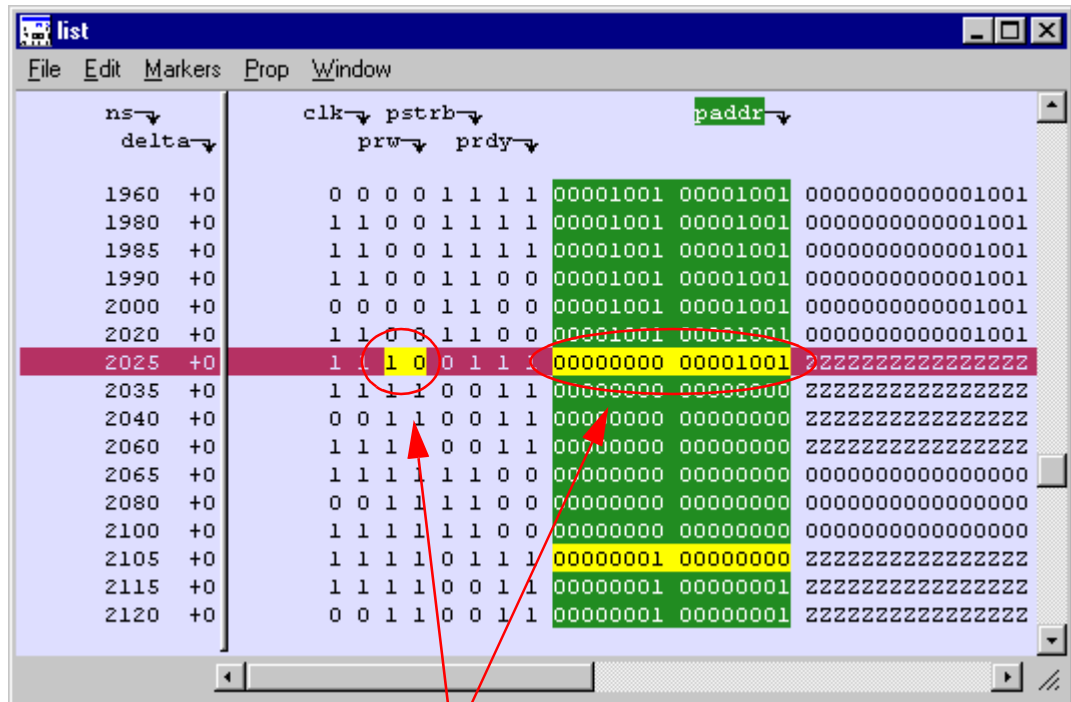
To save the difference information to a text file, select **Compare > Differences > Write Report**.

To save the comparison so it can be reloaded into ModelSim, you must save two files. Select **Compare > Differences > Save** to save the computed differences. Next, select **Compare > Rules > Save** to save the comparison configuration rules. To reload the comparison later, you would start a comparison and then use the **Compare > Reload** command.

Viewing comparison results in the List window

You can also view the results of your waveform comparison in the List window.

- 1 Select **View > List** to open the List window.
- 2 Drag the region from the Compare tab in the Main window to the List window. This will load the compared signals into the List window. Scroll down the window, and you'll see differences shown in yellow.



difference markers

Specifying tolerances

There may be times you want to allow for leading or trailing tolerances in the test dataset signals. You can do this easily by modifying the signal properties of a comparison object in the Wave window.

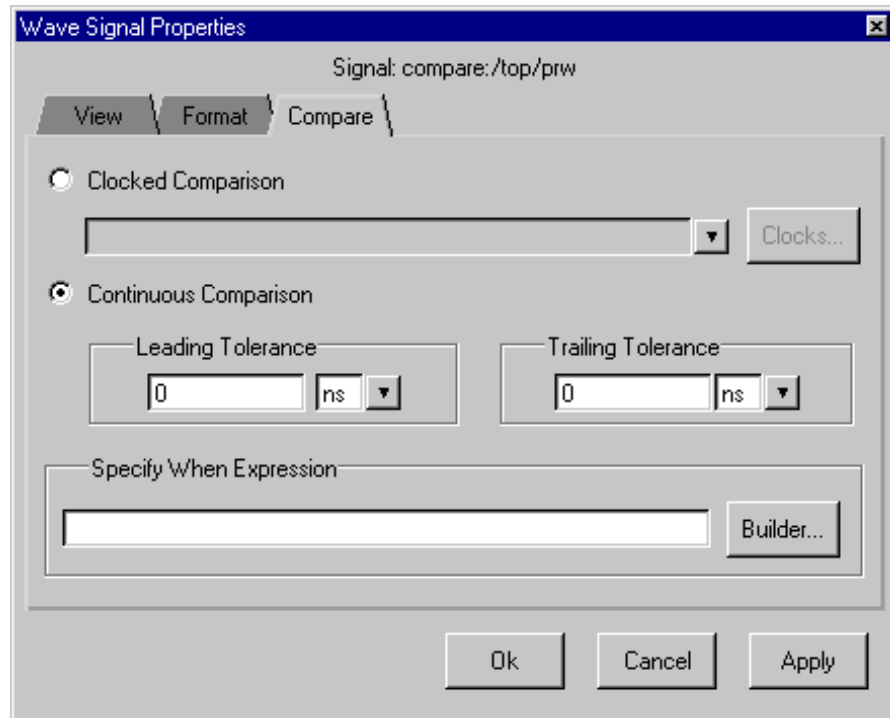
- 1 Click the Find Next Difference icon until you can see the differences at 2025 ns.



(KEYBOARD: Tab)

- 2 Select "compare:/top/prw" in the signals list and then open the Signal Properties dialog. Select the Compare tab.

(MENU: Edit > Signal Properties)



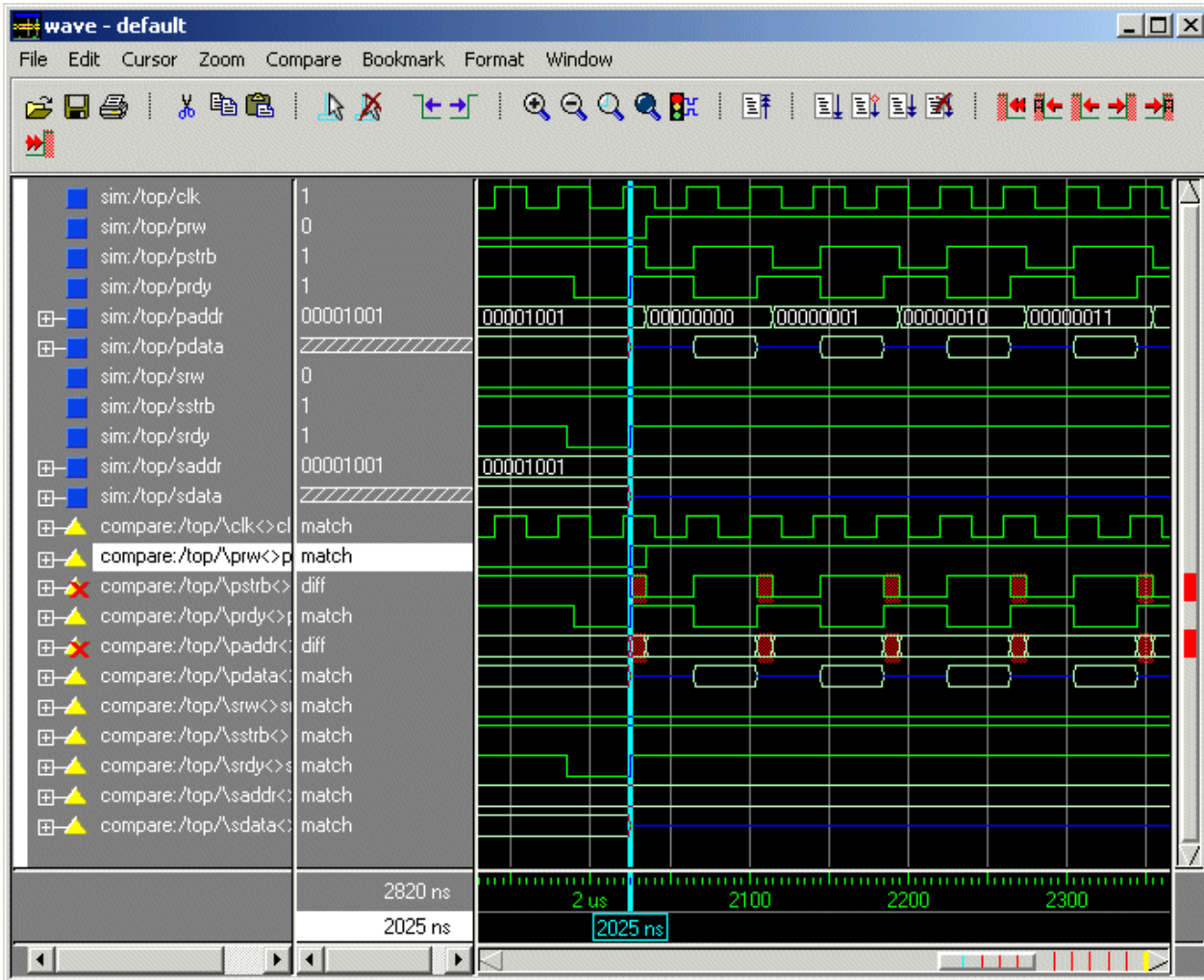
Recall that we delayed the read cycle in *proc.v* by 10 time units. Therefore, if we specify a trailing tolerance of 10 ns, the differences on the comparison object should disappear.

- 3 Specify 10 ns for the Trailing Tolerance and then click OK.

- 4 Rerun the comparison.

(MENU: Compare > Run Comparison)

- Notice that the difference markers have disappeared for the /top/prw comparison object.



- Quit the simulator.

```
quit -f
```

Lesson 13 - Tcl/Tk and ModelSim

The goals for this lesson are:

- Create a "hello world" button widget
- Execute a procedure using a push button
- Simulate an intersection with traffic lights
- Draw a state machine that represents the simulation

This lesson is divided into several Tcl examples intended to give you a sense of Tcl/Tk's function within ModelSim. The examples include a custom simulation interface created with Tcl/Tk (the code is already written).

- ▶ **Note:** You must be using ModelSim SE-VHDL or ModelSim SE/MIXED to complete these exercises.

More information on Tcl/Tk

Sources of information about Tcl include *Tcl and the Tk Toolkit* by John K. Ousterhout, published by Addison-Wesley Publishing Company, Inc., and *Practical Programming in Tcl and Tk* by Brent Welch published by Prentice Hall.

Or, consult one of the following online Tcl references:

- Select **Help > Tcl Man Pages** (Main window) within ModelSim.
- Tcl man pages are also available at: <http://dev.scriptics.com/man/tcl8.1/contents.htm>
- The Model Technology web site lists a variety of Tcl resources: www.model.com/resources/tcltk.asp

How Tcl/Tk works with ModelSim

ModelSim incorporates Tcl as an embedded library package. The Tcl library consists of a parser for the Tcl language, routines to implement the Tcl built-in commands, and procedures that allow Tcl to be extended with additional commands specific to ModelSim.

ModelSim generates Tcl commands and passes them to the Tcl parser for execution. Commands may be generated by reading characters from an input source, or by associating command strings with ModelSim's user interface features, such as menu entries, buttons, or keystrokes.

When the Tcl interpreter receives commands it parses them into component fields and executes built-in commands directly. For commands implemented by ModelSim, Tcl calls back to the application to execute the commands. In many cases commands will invoke recursive invocations of the Tcl interpreter by passing in additional strings to execute (procedures, looping commands, and conditional commands all work in this way).

ModelSim gains a programming advantage by using Tcl for its command language. ModelSim can focus on simulation-specific commands, while Tcl provides many utility commands, graphic interface features, and a general programming interface for building up complex command procedures.

By using Tcl, ModelSim need not re-implement these features, a benefit that allows its graphic interface to remain consistent on all platforms. (The only vestige of the host platform's graphic interface is the window frame manager.)

The custom traffic-light interface

The subject of our main Tcl/Tk lesson is a simple traffic-light controller. The system is comprised of three primary components: a state machine, a pair of traffic lights, and a pair of traffic sensors. The components are described in three VHDL files: `traffic.vhd` (the state machine), `queue.vhd` (the traffic arrival queue) and `tb_traffic.vhd` (the testbench).

You could, of course, simulate this system with *ModelSim*'s familiar interface, but Tcl/Tk provides us the option to try something different. Since we're simulating something most of us have seen and experienced before, we can create an intuitive interface unique to the simulation.

Assumptions

The example assumes that source files were previously compiled. Here's how it works:

VHDL source files describe the system	Tcl procedures create and connect the interface, plus the source files, to <i>ModelSim</i>	<i>ModelSim</i> commands are run via the new interface using the Tcl procedures
	<code>draw_intersection</code>	
<code>traffic.vhd</code> <code>queue.vhd</code> <code>tb_traffic.vhd</code>	<code>connect_lights</code>	<code>vsim -lib vhdl/work tb_traffic</code> <code>examine -value <light_timing></code>
	<code>draw_queues</code>	
	<code>draw_controls</code>	<code>force -freeze \$var \$val ns</code>

The result is a traffic intersection interface similar to this illustration:

wm widget
Calls to the operating system window manager to create the "traffic" window.

frame and scale widget
A scale widget within a frame widget creates an analog entry device for a minimum to a maximum value and invokes the force command

label widget
A static label is added to the end of the connect_lights procedure to indicate connection to the simulator.

canvas widget
The background, lines and traffic lights are created with the canvas widget.

button widgets
Each button invokes the indicated run or break command.

Tk widgets

The intersection illustration points out several Tcl/Tk "widgets." A widget is simply a user interface element, like a menu or scrolled list. Tk widgets are referenced within Tcl procedures to create graphic interface objects. The Tk tool box comes with several widgets, additional widgets can be created using these as a base.

Controlling the simulation

The components of the intersection interface have the following effect within *ModelSim*:

Intersection control used	Effect in <i>ModelSim</i>
Run 1000 button	invokes the run command for 1000 ns
Run Forever button	invokes the run -all command
Break button	invokes the break command
light timing control	invokes the force command with the arguments for the indicated signal and time
arrival time control	invokes the force command with the arguments for the indicated direction and time
waiting queue	any time you change a control the examine command is invoked to display the value of the waiting queue

Saving time

Since several intersection controls invoke a command and arguments with a single action (such as the movement of a slider), this custom interface saves time compared to invoking the commands from the command line or *ModelSim* menus.

Copies of the original example files

Additional copies of the Tcl example files from these exercises are located in the `<install_dir>\modeltech\examples\tcl_tutorial\originals` directory.

Solutions to the examples

Throughout the traffic intersection examples you will be modifying Tcl files to complete the final intersection. You will find a completed set of intersection examples ready-to-run in the `tcl_tutorial\solutions` directory. Invoke these commands from the *ModelSim* prompt to run the intersection:

```
cd solutions
do traffic.do
```

Viewing files

If you would like to view the source for any of the Tcl files in our examples, use the **notepad** command at either the *ModelSim* or VSIM prompt.

```
notepad <filename>
```

Most files are opened in read-only mode by default; you can edit the file by deselecting **read only** from the notepad **Edit** menu.

The Tcl source command

The Tcl **source** command reads the Tcl file into the Tcl interpreter, which parses the procedures for use within the current environment. Once sourced, a Tcl procedure can be called from the *ModelSim* prompt as shown in the syntax below. *ModelSim* executes the instructions within the procedure.

Syntax

```
source <tcl filename>
<tcl procedure name>
```

Arguments

```
<tcl filename>
```

The Tcl file read into the *ModelSim* Tcl interpreter with the source command.

```
<tcl procedure name>
```

The Tcl procedure defined within <tcl filename>, called from the *ModelSim* prompt, and executed by *ModelSim*.

The *traffic.do* file is a good example of the **source** command syntax (the file is a macro that runs the traffic light simulation). View it with Notepad:

```
notepad traffic.do
```

Shortcuts

To save some typing, copy the commands from the PDF version of these instructions and paste them at the *ModelSim* prompt. Paste with the right (2 button mouse), or middle (3 button mouse). You can also select a *ModelSim* or VSIM prompt from the Main transcript to paste a previous command to the current command line.

Make a transcript DO file

You can rerun the commands executed during the current session with a Do file created from the Main transcript. Make the DO file by saving the transcript with the **File > Save Transcript As** menu selection at any time during the exercises. Run the DO file to repeat the commands (do <do filename>).

Initial setup

▲ **Important:** These steps must be completed before running the Tcl examples.

- 1 Create, and change to a new working directory for the Tcl/Tk exercises. Copy the lesson files in the following directory (include all subdirectories and files) to your new directory:

```
<install_dir>\modeltech\examples\tcl_tutorial
```

- 2 Make the new directory the current directory, then invoke *ModelSim*:

for UNIX

```
vsim
```

for Windows (from a shortcut or Start > Run, etc.)

```
modelsim.exe
```

- 3 At the *ModelSim* prompt, create a **work** library in the */vhdl* directory:

```
vlib vhdl/work
```

- 4 Map the **work** library.

```
vmap work vhdl/work
```

- 5 Compile the VHDL example files with these commands (or the Compile dialog box):

```
vcom vhdl/traffic.vhd  
vcom vhdl/queue.vhd  
vcom vhdl/tb_traffic.vhd
```

Example 1 - Create a "Hello World" button widget

Before you begin the examples make sure you have completed "[Initial setup](#)" (T-115).

In this example you will study a "hello world" button that prints a message when pressed.

- 1 Source the Tcl file from the ModelSim prompt:

```
source hello.tcl
```

then run the procedure defined within *hello.tcl*:

```
hello_example
```

The file *hello.tcl* was read into the ModelSim Tcl interpreter. The instructions in the *hello_example* procedure were then executed by ModelSim, and "Hello World" was printed to the Main transcript (or invoking shell on UNIX). Selecting the button will print the message again.

You've just created your first top-level widget!

- 2 Invoke the *hello_example* procedure again and notice how the new button replaces the original button. The procedure destroyed the first button and created the new one. Get a closer look at the source Tcl file with the **notepad**:

```
notepad hello.tcl
```

Close the *hello_example* window when you're done.

Example 2 - Execute a procedure using a push button

Before you begin this example make sure you have completed "[Initial setup](#)" (T-115).

This example will display all of the gif images in the images directory. Each button has a binding attached to it for "enter" events, and a binding for a mouse button press. When the mouse enters the button graphic, the image file name is printed to the Main window (or invoking shell on UNIX). When the mouse button is pushed, its "widget" name will be printed to the Main window (or invoking shell on UNIX).

- 1 Build an image viewer by invoking this command, and calling this procedure:

```
source images.tcl
image_example
```

- 2 Drag the mouse across the buttons and notice what happens in the Main transcript (or invoking shell on UNIX).

Push one of the buttons; you will see an error dialog box. You can solve this problem by modifying the *images.tcl* file.

- 3 To view the source file press the **See Source Code** button at the bottom of the image display or invoke **notepad** at the ModelSim prompt:

```
notepad images.tcl
```

You'll find that the *pushme* procedure is missing; it's commented out in *images.tcl*.

- 4 Search for "proc push" using the **Edit > Find** menu selection in the notepad.

Remove the comments (the "#" symbols) to return the function to your source, use **File > Save** to save the changes, then close the image window with the **Destroy** button.

- 5 Once the *pushme* procedure is in place it will print its one parameter, the object name, to the transcript.

After you have added the *pushme* procedure to your source, you need to resource and rerun the Tcl procedure with these commands (use the up arrow to scroll through the commands or do !source):

```
source images.tcl
image_example
```

Press all the buttons and notice the object names in the Main transcript. Close the image example window when you're done.

Example 3 - Simulate an intersection with traffic lights

In this example you'll simulate an intersection with traffic lights. The simulation interface you create allows you to run "what if" scenarios efficiently.

Introduction of the traffic intersection widget

This portion of our example introduces the traffic intersection widget. You'll add other widgets to the intersection to create a custom traffic simulation environment.

Once again, make sure you have completed "[Initial setup](#)" (T-115) before working this example.

- 1 Draw the intersection by invoking this command and procedure at the *ModelSim* prompt:

```
source intersection.tcl
draw_intersection
```

- 2 From the *ModelSim* prompt, use the procedure `set_light_state` to change the color of the lights:

```
set_light_state green .traffic.i.ns_light
set_light_state green .traffic.i.ew_light
```

You can use the Copy and Paste buttons on the Main toolbar to help build instructions from previous commands.

- 3 View the source code with this command at the *ModelSim* prompt:

```
notepad intersection.tcl
```

You can locate the `set_light_state` procedure with **Edit > Find** from the Notepad menu (the procedure is located toward the middle of the file).

Connect traffic lights to the simulation

Using the intersection widget, you will add *when* statements to connect the lights to the real simulation. Once the connection is made, you will simulate the traffic light controller and watch the lights change.

We'll use *ModelSim when* statements to condition the simulation to call our Tcl program when a desired simulation condition happens.

For our example, the desired condition is the state of the lights. Whenever the lights in the simulation change states, we want to change the color of the lights on the screen.

- 4 Load the VHDL libraries you compiled in preparation for these examples using this command at the *ModelSim* prompt:

```
vsim tb_traffic
```

Be sure you invoke this command before the start of the `connect_lights` procedure, if you don't load the libraries, you won't have a design to simulate.

- 5 Connect the lights to the simulation with this command and procedure:

```
source lights.tcl
connect_lights
```

Try running the simulation now; select either run button on the intersection. Select **Break** if you used the **Run Forever** button. Notice how the Source window opens and indicates the next line to be executed. (If the simulator is not evaluating an executable process when the break occurs, the Source window will not open.) Only the East/West lights are working. You can make both lights work by editing the *lights.tcl* file.

- 6 Edit *lights.tcl* with the **notepad** to add a *when* statement for the North/South light.

```
notepad lights.tcl
```

You need to add this because the current statement is for the East/West light only. You'll find the solution commented. (Remember to change the read-only status of the file so you can edit it.)

You'll find the code commented-out toward the end of the file (use **Edit >Find** and look for *light_ns*).

- 7 After you have made the changes, reload and run the simulation again.

```
source lights.tcl
connect_lights
```

Both lights are now working.

- **Note:** Remember, if you need to return to the original Tcl files (maybe you've edited the file and it doesn't work right) you'll find the files in the *tcl_tutorial\originals* directory.

Add widgets to display simulation information

Running the lights may be interesting, but not very useful - let's add some displays that will tell us what's happening to the cars at the intersection.

Now you will add queue widgets to display the sum of the length of each pair of queues as we simulate.

- 8 The East/West widget for displaying the total East/West queue length is already provided. Let's edit the source to add a display for the North/South direction. Use the **notepad**:

```
notepad queues.tcl
```

The solution is commented out in *queues.tcl*.

The Queue Display widget consists of an enclosing frame with two label widgets. The first label is a simple text string. The second label is the value of the queue length. The text in the second label will be updated whenever the queue lengths change.

- 9 After you have added your North/South widget, run your program by invoking this command:

```
source queues.tcl
draw_queues
```

According to the traffic indicators, the cars are leaving the intersection at the same rate. That seems fair, but if you are designing an intersection that responds to the traffic flow into the intersection you might want to change the light cycles. Perhaps one of the directions has more incoming traffic than the other.

Adding controls, in the form of scale widgets, allows you to quickly change the assumptions about traffic flow into the intersection.

Add "scale" widgets to control the simulation

Next you will add Tk "scale" widgets that will control the arrival rates and the length of the lights.

- 10** The East/West widget for controlling the East/West queue inter-arrival time is provided. You'll edit the source code to add controls for the North/South direction. Use this command:

```
notepad controls.tcl
```

You can remove the comments in the code to make this change.

Similarly, add the North/South widget for controlling the length of the lights. The East/West widget for light control is provided. (You can remove the comments in the code to make this change as well.)

These control widgets are implemented using the Tk "scale" widgets, enclosed in a frame.

When the value of the scale widget changes, it calls the command specified with the **-command** option on each scale.

- 11** After you have added your North/South widgets, run your program with this command:

```
source controls.tcl
draw_controls
```

Now you have a complete intersection interface. Try the run buttons and the slider scales.

You can view the simulation with ModelSim's GUI. Check the Source window to view the VHDL files, and add signals to a Wave window (**add wave ***).

You can also change the run length in the Main window. Try using the Run buttons in the Main window and the intersection window.

Keep the intersection simulation running to complete the next example. If you want to recreate the final intersection environment quickly, invoke these commands from the ModelSim prompt (after "Initial setup" (T-115)):

```
cd solutions
vmap work work
do traffic.do
```

Example 4 - Draw a state machine that represents the simulation

In this final example you will draw a state machine representing the simulation, and connect it to the state signal inside the traffic light controller. Each transition that the controller makes is displayed as it happens.

The intersection environment from the previous example needs to be running for this example. To get it running quickly, invoke these commands from the *ModelSim* prompt (after "Initial setup" (T-115)).

```
cd solutions
do traffic.do
```

- 1 Run the state machine with these commands:

```
source state-machine.tcl
draw_state_machine
```

Let's make some changes to the light colors and transition arrows.

- 2 Open the source file with this command:

```
notepad state-machine.tcl
```

Note the "*ModelSim* EXAMPLE part 1" comments in the file. You can change "both_red" state coordinates from $x = 125$ and $y = 50$ to any coordinates. (You may need to uncheck the **read only** selection in the Edit menu before making changes.)

- 3 Note the "*ModelSim* EXAMPLE part 2" comments in the file. You can change the transition arrow coordinates to correspond with the new "both_red" state coordinates.
- 4 Note the "*ModelSim* EXAMPLE part 3" comments in the file. Change the active color from "black" to "purple".
- 5 Reuse the original commands when you're ready to run the state machine (remember, to copy a previous command to the current command line, select the previous *ModelSim* prompt):

```
source state-machine.tcl
draw_state_machine
```

Notice the changes. Try some additional changes if you wish.

This is the end of the Tcl/Tk examples. Continue to modify and test the examples if you wish; you can recover the original files at any time in the *tcl_tutorial/originals* directory.

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